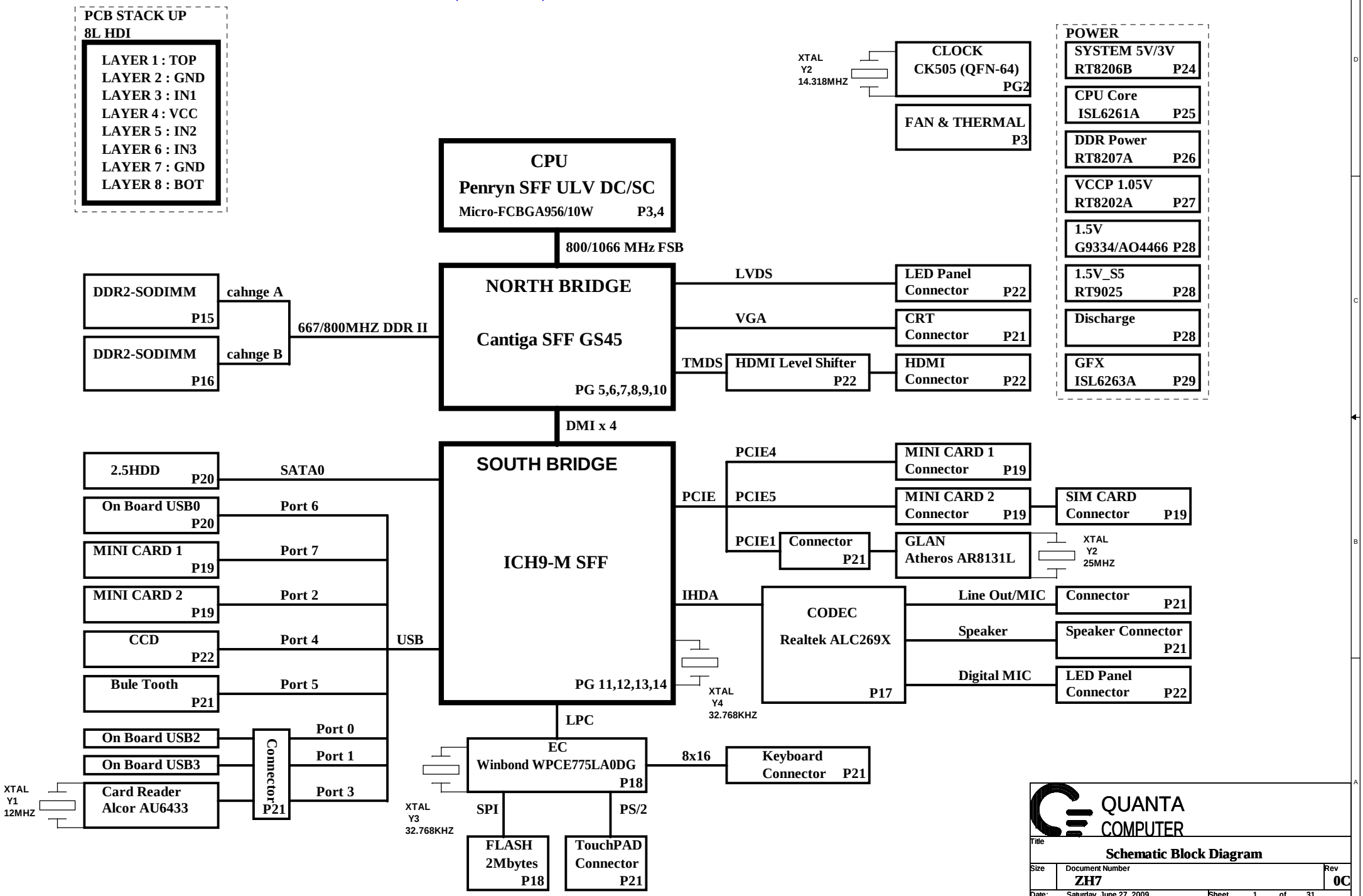
JM11_MS (ZH7) BLOCK DIAGRAM



QUANTA COMPUTER

Title	Schematic Block Diagram	
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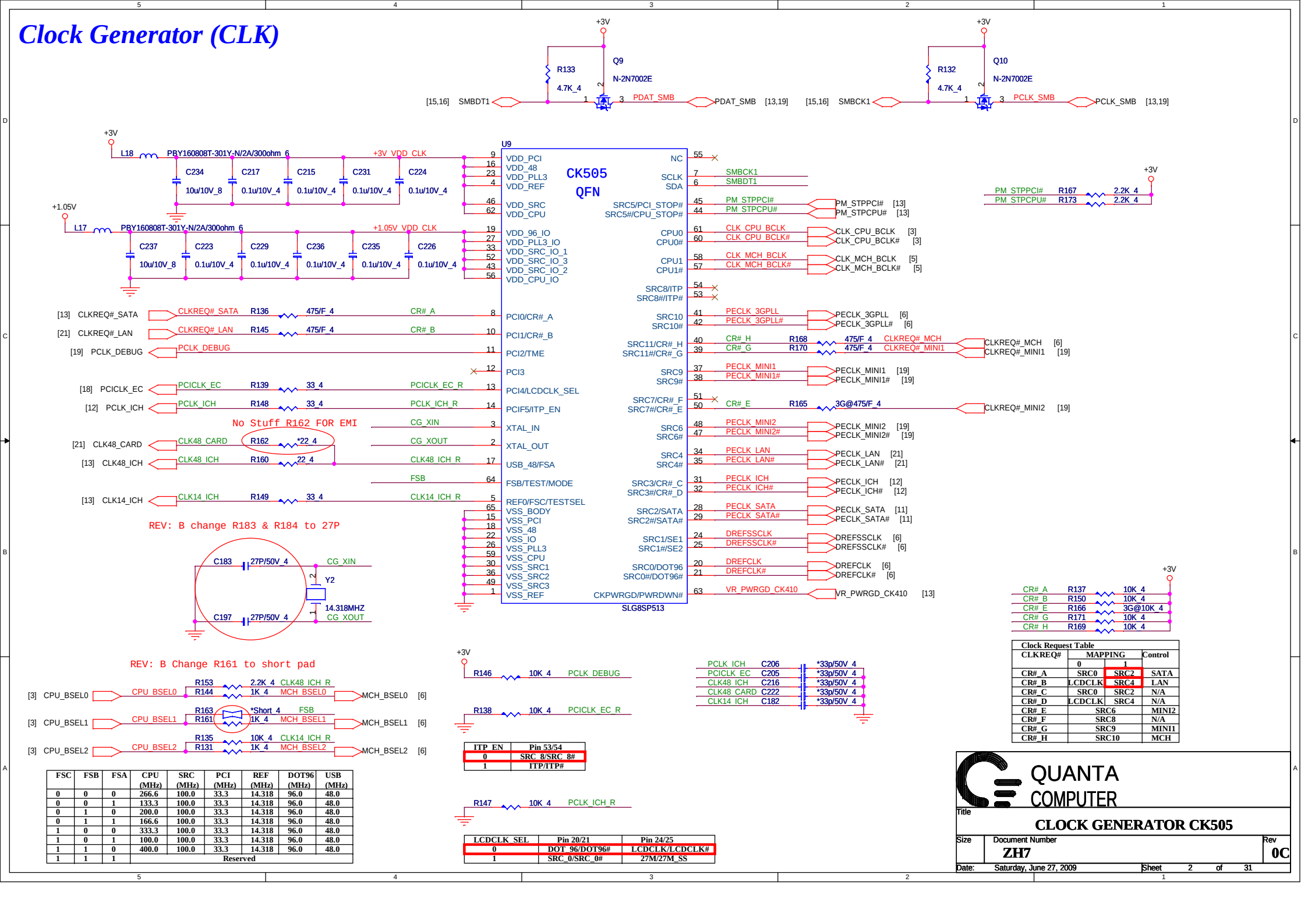
Clock Generator (CLK)



FSC	FSB	FSA	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT96 (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0
1	1	1	Reserved					

ITP_EN	Pin 53/54
0	SRC_8/SRC_8#
1	ITP/ITP#

LCDCLK_SEL	Pin 20/21	Pin 24/25
0	DOT_96/DOT96#	LCDCLK/LCDCLK#
1	SRC_0/SRC_0#	27M/27M_SS

Clock Request Table			
CLKREQ#	MAPPING		Control
	0	1	
CR#_A	SRC0	SRC2	SATA
CR#_B	LCDCLK	SRC4	LAN
CR#_C	SRC0	SRC2	N/A
CR#_D	LCDCLK	SRC4	N/A
CR#_E	SRC6		MINI2
CR#_F	SRC8		N/A
CR#_G	SRC9		MINI1
CR#_H	SRC10		MCH

QUANTA COMPUTER

Title	CLOCK GENERATOR CK505	
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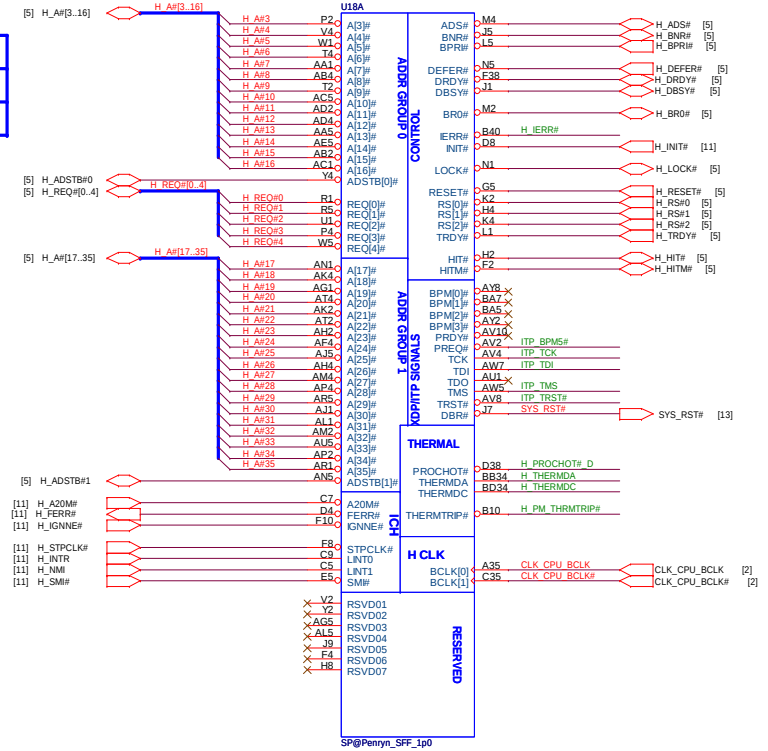
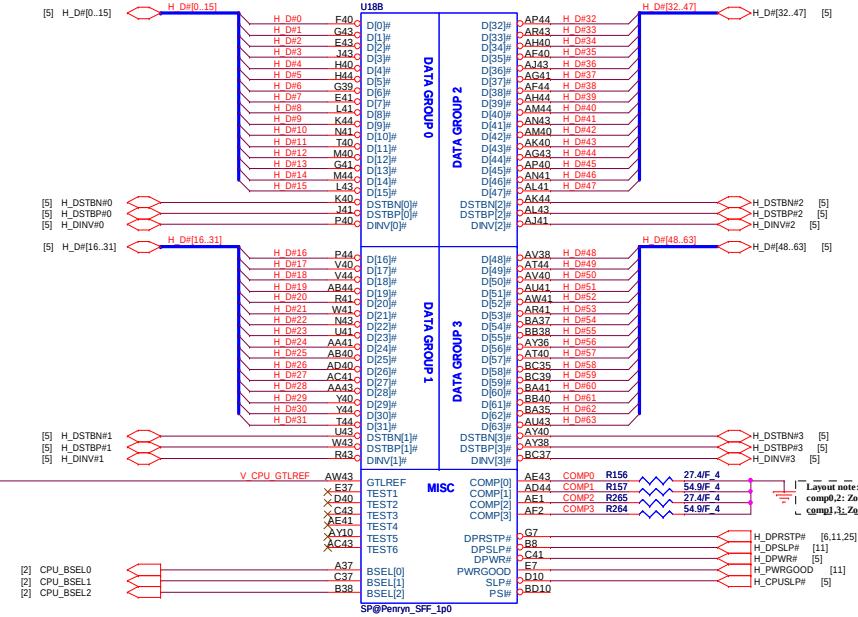
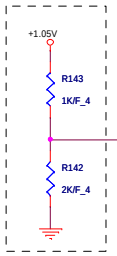
Penryn SFF - Host Bus (CPU)

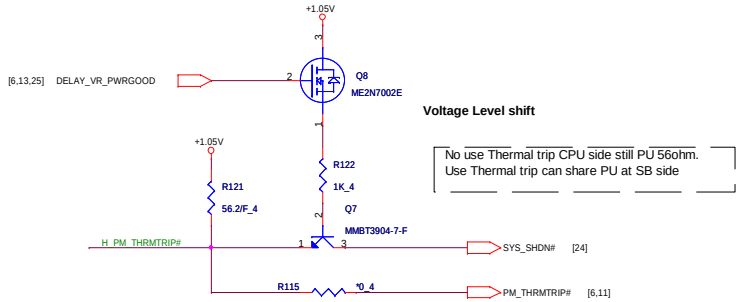
1.2G	AJSLGAMVT02
1.4G	AJSLGFMTT00

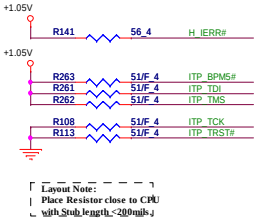


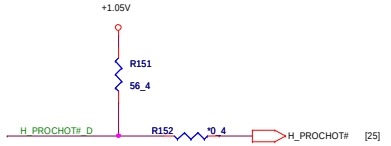




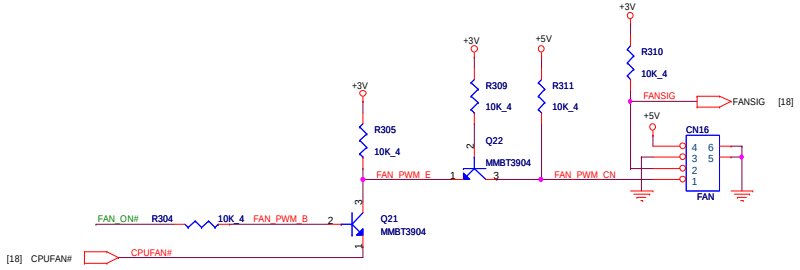
Layout Note:
Place voltage divider
within 0.5" of GTLREF pin



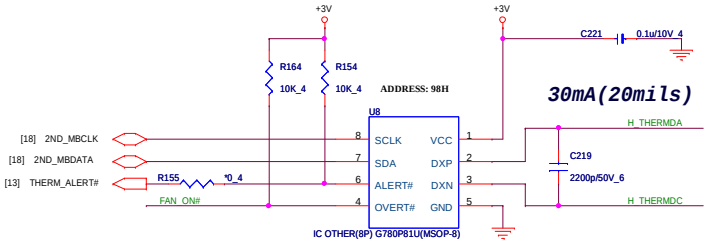




CPU FAN CTRL(THM)



CPU Thermal Monitor(THM)



QUANTA COMPUTER

Title	Penryn SFF (Host Bus)/FAN/Thermal	
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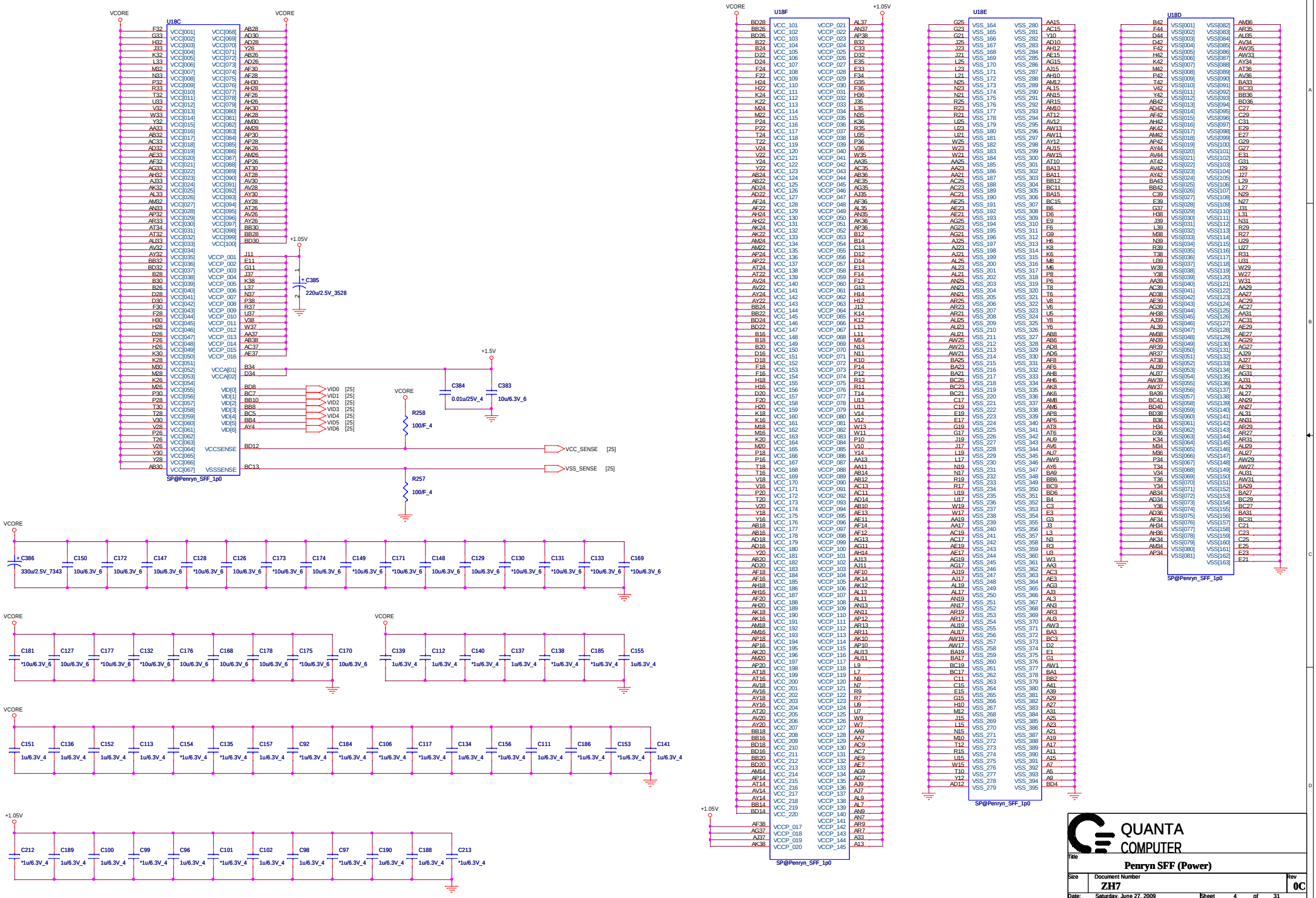
Penryn SFF - Power (CPU)



Title	Penryn SFF (Power)	
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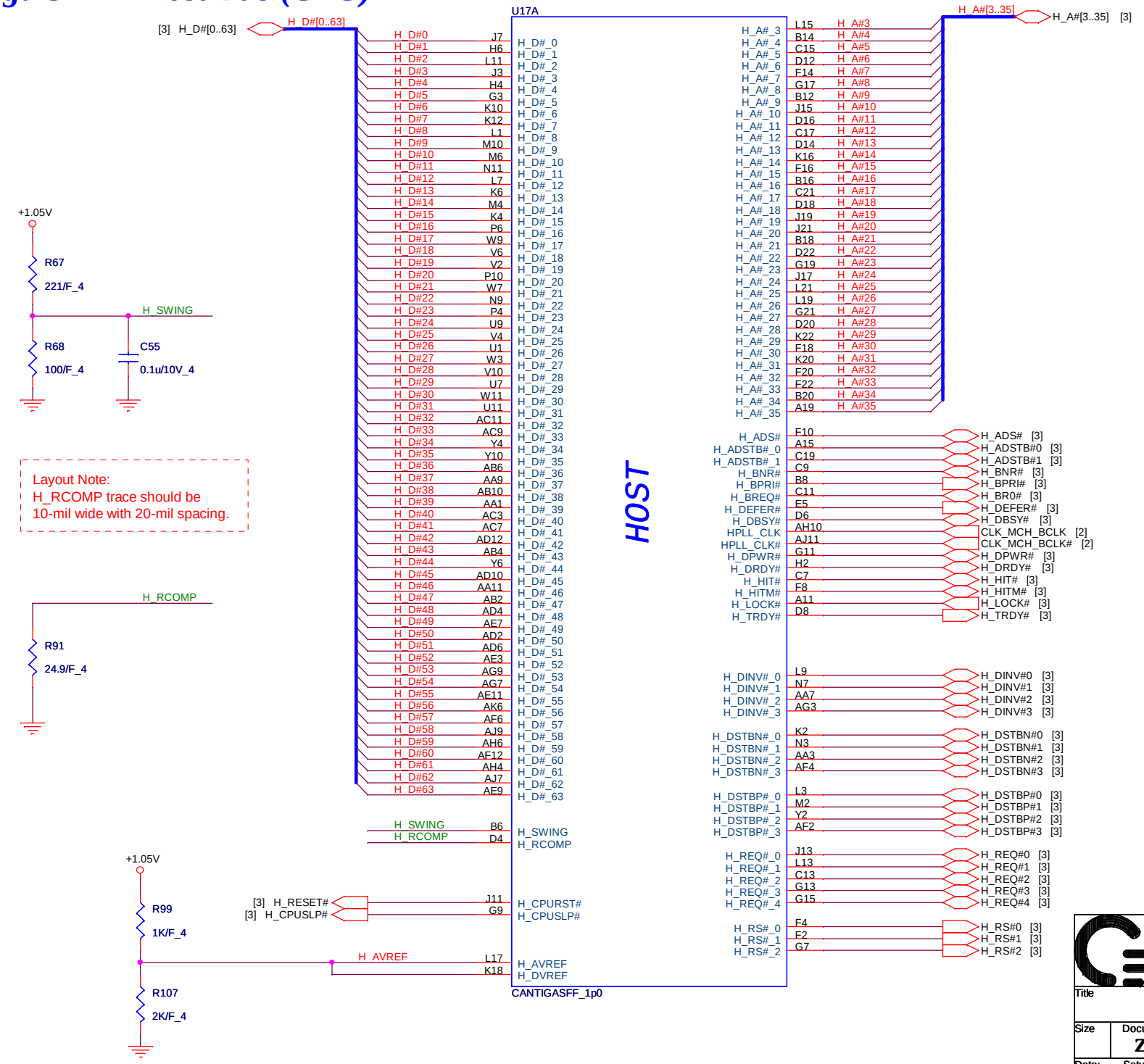
QUANTA COMPUTER

Cantiga SFF - Host Bus (CLG)



QUANTA COMPUTER

Title: Cantiga SFF (Host Bus)		
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Cantiga SFF - DMI/VGA (CLG)

Intel GS40/GS45 Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Other = Reserved
CFG4:3	Reserved	
CFG5	DMI x2 Select	1 = DMI x 4 0 = DMI x2
CFG6	ITPM Host Interface	1 = ITPM disabled 0 = ITPM enabled
CFG7	Intel Management Engine Crypto Strap	1 = Intel Management Engine Crypto TLS cipher suite with confidentiality 0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
CFG8	Reserved	
CFG9	PCIE Graphics Lane	1 = Normal operation : Lane Numbered in Order 0 = Reverse Lanes
CFG10	PCIE Loopback enable	1 = Disabled 0 = Enabled
CFG11	Reserved	
CFG12	ALLZ	1 = Disabled 0 = ALLZ mode enabled
CFG13	XOR	1 = Disabled 0 = XOR mode enabled
CFG14	Reserved	
CFG15	Reserved	
CFG16	FSB Dynamic ODT	1 = Dynamic ODT enabled 0 = Dynamic ODT disabled
CFG17	Reserved	
CFG18	Reserved	
CFG19	DMI Lane Reversal	1 = Reverse Lanes 0 = Normal operation : Lane Numbered in Order
CFG20	Digital DisplayPort (SDVO/DP/iHDMI) Concurrent with PCIE	1 = Digital DisplayPort (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port 0 = Digital DisplayPort (SDVO/DP/iHDMI) or PCIE are operational
SDVO_CTRLDATA	SDVO Present	1 = SDVO/HDMI/DP interface enabled 0 = No SDVO/HDMI/DP interface disabled
L_DDC_DATA	Local Flat Panel (LFP) Present	1 = LFP Card Present: PCIE disabled 0 = LFP Disable
DDPC_CTRLDATA	Digital Display Present	1 = Digital display (iHDMI/DP) devide present 0 = Digital display (iHDMI/DP) interface absent

- The recommended pull-up resistor value is 4.02 kΩ ±1%
- The recommended pull-down resistor value is 2.21 kΩ ±1%.

U17B

RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
PM
GRAPHICS VID
ME
NC
MISC
HDA

CANTIGASFF_1p0

U17C

CANTIGASFF_1p0

PCI-EXPRESS GRAPHICS
DMI
VGA
CRT
LVDS
HDMI Port B

CRT setting

LVDS setting

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

Check list note : CL_REF=0.35V

REV: B Change R254 to short pad

QUANTA COMPUTER

Title: Cantiga SFF (DMI/VGA)

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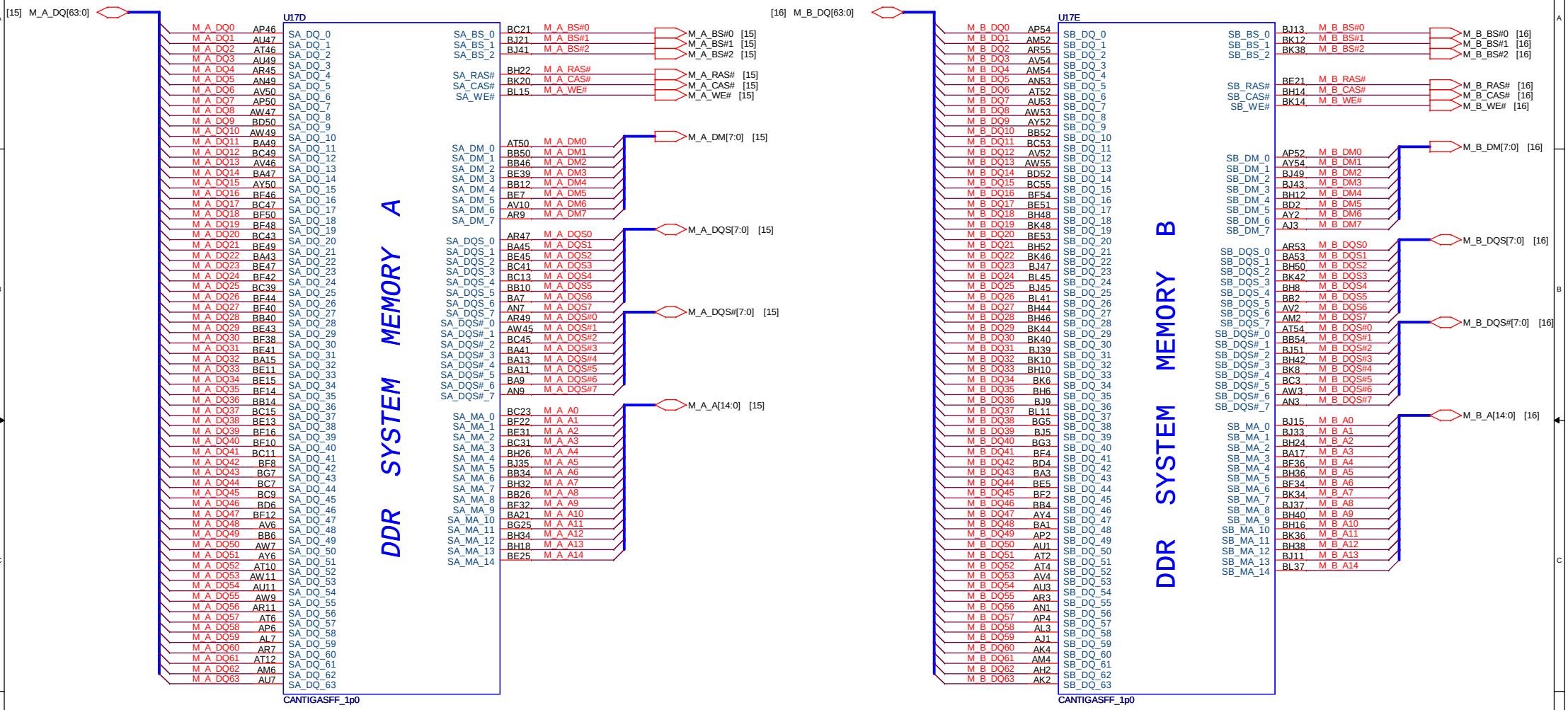
Cantiga SFF - DDRII (CLG)



QUANTA COMPUTER

Title: Cantiga SFF (DDRII)

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Cantiga SFF - VCC/NCTF (CLG)

Ivcc internal VGA 2.4A
(Shape or 140mils)

DDR2-667 2.6A
DDR2-800 3A
(Shape or 140mils)

UMA 9.6A(GM45)
(Plane or shape)

VCC 2200mA

U17F

+1.05V

VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12
VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34
VCC_35 VCC_36
VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61

VCC CORE

POWER

VCC NCTF

+1.05V

VCC_NCTF_1 AT38
VCC_NCTF_2 AR38
VCC_NCTF_3 AN38
VCC_NCTF_4 AM38
VCC_NCTF_5 AL38
VCC_NCTF_6 AG38
VCC_NCTF_7 AE38
VCC_NCTF_8 AA38
VCC_NCTF_9 Y38
VCC_NCTF_10 W38
VCC_NCTF_11 U38
VCC_NCTF_12 T38
VCC_NCTF_13 R38
VCC_NCTF_14 AT37
VCC_NCTF_15 AR37
VCC_NCTF_16 AN37
VCC_NCTF_17 AM37
VCC_NCTF_18 AL37
VCC_NCTF_19 AJ37
VCC_NCTF_20 AH37
VCC_NCTF_21 AG37
VCC_NCTF_22 AE37
VCC_NCTF_23 AD37
VCC_NCTF_24 AC37
VCC_NCTF_25 AA37
VCC_NCTF_26 Y37
VCC_NCTF_27 W37
VCC_NCTF_28 U37
VCC_NCTF_29 T37
VCC_NCTF_30 R37
VCC_NCTF_31 AT35
VCC_NCTF_32 AR35
VCC_NCTF_33 U35
VCC_NCTF_34 AT34
VCC_NCTF_35 AR34
VCC_NCTF_36 U34
VCC_NCTF_37 T34
VCC_NCTF_38 R34

CANTIGASFF_1p0

U17G

+1.8VSUS

+VCC_SM_BB36 BB36
+VCC_SM_BE35 BE35
C198 0.1u/10V_4
C204 0.1u/10V_4

VCC_SM :3000mA

+VCC_SM_BC29 BC29
C200 0.1u/10V_4

+VCC_SM_BF24 BF24
+VCC_SM_BL19 BL19
+VCC_SM_BB16 BB16
C203 0.1u/10V_4
C379 0.1u/10V_4
C201 0.1u/10V_4

VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33

VCC SM

POWER

+VGFX

VCC_AXG_1 VCC_AXG_2 VCC_AXG_3 VCC_AXG_4 VCC_AXG_5 VCC_AXG_6 VCC_AXG_7 VCC_AXG_8 VCC_AXG_9 VCC_AXG_10 VCC_AXG_11 VCC_AXG_12 VCC_AXG_13 VCC_AXG_14 VCC_AXG_15 VCC_AXG_16 VCC_AXG_17 VCC_AXG_18 VCC_AXG_19 VCC_AXG_20 VCC_AXG_21 VCC_AXG_22 VCC_AXG_23 VCC_AXG_24 VCC_AXG_25 VCC_AXG_26 VCC_AXG_27 VCC_AXG_28 VCC_AXG_29 VCC_AXG_30 VCC_AXG_31 VCC_AXG_32 VCC_AXG_33 VCC_AXG_34 VCC_AXG_35 VCC_AXG_36 VCC_AXG_37 VCC_AXG_38 VCC_AXG_39 VCC_AXG_40 VCC_AXG_41 VCC_AXG_42 VCC_AXG_43 VCC_AXG_44 VCC_AXG_45 VCC_AXG_46 VCC_AXG_47 VCC_AXG_48 VCC_AXG_49 VCC_AXG_50 VCC_AXG_51 VCC_AXG_52 VCC_AXG_53 VCC_AXG_54 VCC_AXG_55 VCC_AXG_56 VCC_AXG_57 VCC_AXG_58 VCC_AXG_59 VCC_AXG_60 VCC_AXG_61

VCC_AXG 7700mA

VCC_AXG_SENSE
VSS_AXG_SENSE

VCC GFX

VCC GFX NCTF

+VGFX

VCC_AXG_NCTF_1 T32
VCC_AXG_NCTF_2 U31
VCC_AXG_NCTF_3 T31
VCC_AXG_NCTF_4 R31
VCC_AXG_NCTF_5 U29
VCC_AXG_NCTF_6 T29
VCC_AXG_NCTF_7 R29
VCC_AXG_NCTF_8 U28
VCC_AXG_NCTF_9 U27
VCC_AXG_NCTF_10 T27
VCC_AXG_NCTF_11 R27
VCC_AXG_NCTF_12 U25
VCC_AXG_NCTF_13 T25
VCC_AXG_NCTF_14 R25
VCC_AXG_NCTF_15 U24
VCC_AXG_NCTF_16 U22
VCC_AXG_NCTF_17 T22
VCC_AXG_NCTF_18 R22
VCC_AXG_NCTF_19 U21
VCC_AXG_NCTF_20 T21
VCC_AXG_NCTF_21 R21
VCC_AXG_NCTF_22 AM19
VCC_AXG_NCTF_23 AL19
VCC_AXG_NCTF_24 AH19
VCC_AXG_NCTF_25 AG19
VCC_AXG_NCTF_26 AE19
VCC_AXG_NCTF_27 AD19
VCC_AXG_NCTF_28 AC19
VCC_AXG_NCTF_29 W19
VCC_AXG_NCTF_30 U19
VCC_AXG_NCTF_31 AM18
VCC_AXG_NCTF_32 AL18
VCC_AXG_NCTF_33 AJ18
VCC_AXG_NCTF_34 AH18
VCC_AXG_NCTF_35 AG18
VCC_AXG_NCTF_36 AE18
VCC_AXG_NCTF_37 AD18
VCC_AXG_NCTF_38 AC18
VCC_AXG_NCTF_39 AA18
VCC_AXG_NCTF_40 Y18
VCC_AXG_NCTF_41 W18
VCC_AXG_NCTF_42 U18
VCC_AXG_NCTF_43 T18
VCC_AXG_NCTF_44 R18

VCC_AXG_62 AJ16
VCC_AXG_63 AH16
VCC_AXG_64 AD16
VCC_AXG_65 AC16
VCC_AXG_66 AA16
VCC_AXG_67 U16
VCC_AXG_68 T16
VCC_AXG_69 R16
VCC_AXG_70 AM15
VCC_AXG_71 AL15
VCC_AXG_72 AJ15
VCC_AXG_73 AH15
VCC_AXG_74 AG15
VCC_AXG_75 AE15
VCC_AXG_76 AA15
VCC_AXG_77 Y15
VCC_AXG_78 W15
VCC_AXG_79 U15
VCC_AXG_80 T15

VCC GFX

+VGFX R123 12@10/F_4
R117 12@10/F_4

Differential routing
[29] GFX_VCCSENSE AG13
[29] GFX_VSSSENSE AE13

VCC SM LF

VCC_SM_LF1 AU45 VCCSM_LF1
VCC_SM_LF2 BF52 VCCSM_LF2
VCC_SM_LF3 BB38 VCCSM_LF3
VCC_SM_LF4 BA19 VCCSM_LF4
VCC_SM_LF5 BE9 VCCSM_LF5
VCC_SM_LF6 AU9 VCCSM_LF6
VCC_SM_LF7 AL9 VCCSM_LF7

10mil

C165 0.1u/10V_4
C191 0.1u/10V_4
C210 0.22u/10V_4
C202 0.22u/10V_4
C220 0.47u/6.3V_4
C381 1u/10V_6
C382 1u/10V_6

+VGFX
R119 12@0_8
R120 12@0_8

+1.05V
C179 0.1u/10V_4
C115 0.22u/10V_4
C145 0.22u/10V_4
C196 *10u/6.3V_8
C207 *220u/2.5V_3528

Layout Note:
Inside GMCH cavity.

+1.8VSUS
C209 0.1u/10V_4
C211 10u/6.3V_8
C214 10u/6.3V_8

+VGFX
C108 0.47u/6.3V_4
C163 *1u/16V_6
C162 10u/6.3V_6
C123 10u/6.3V_8
C114 0.1u/10V_4
C109 0.1u/10V_4

+VGFX
C83 *220u/2.5V_3528
C125 220u/2.5V_3528

Close to GMCH

Layout Note:
370 mils from edge.

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

CANTIGASFF_1p0

QUANTA COMPUTER

Title	Cantiga SFF (VCC/NCTF)	
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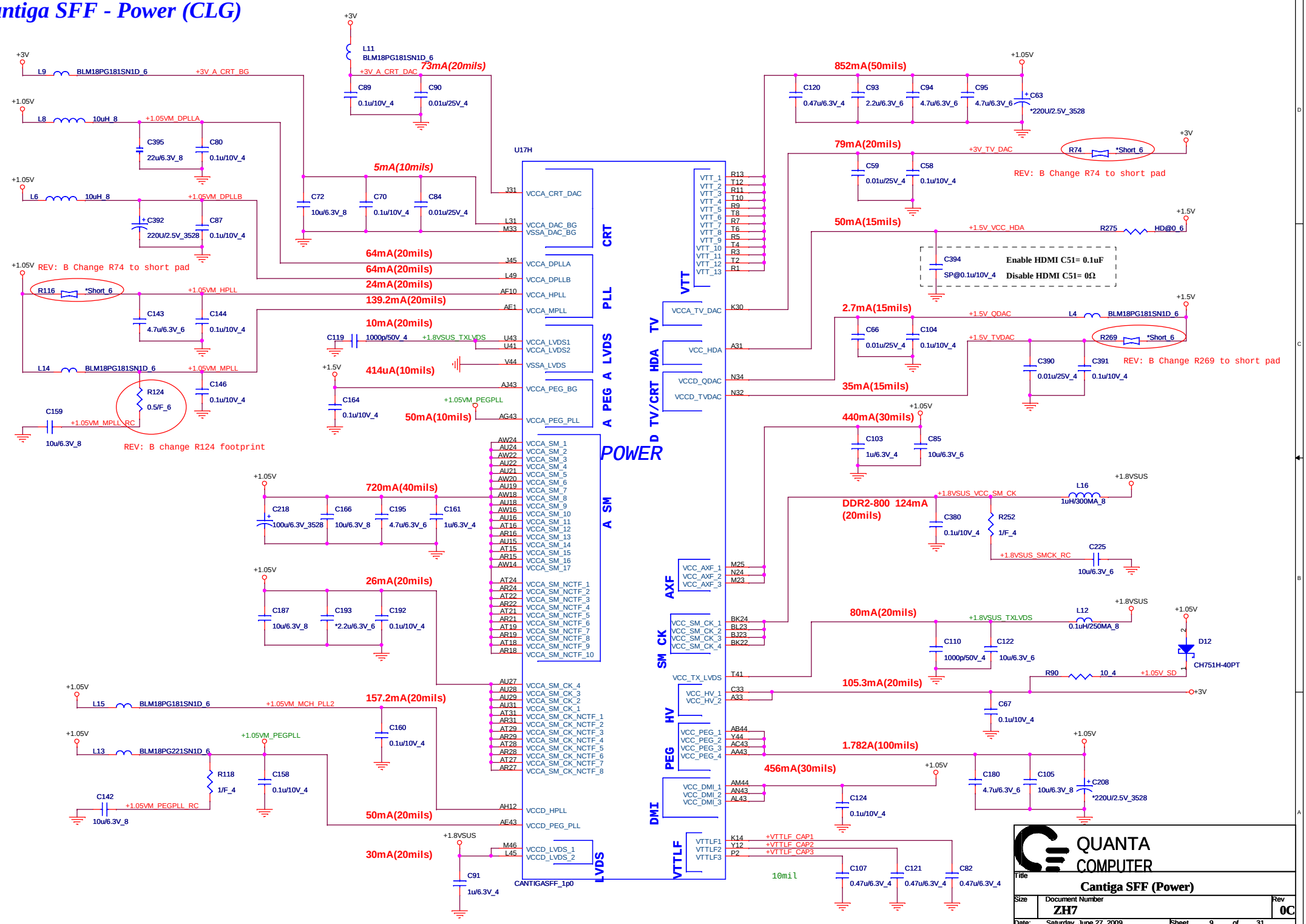
Cantiga SFF - Power (CLG)



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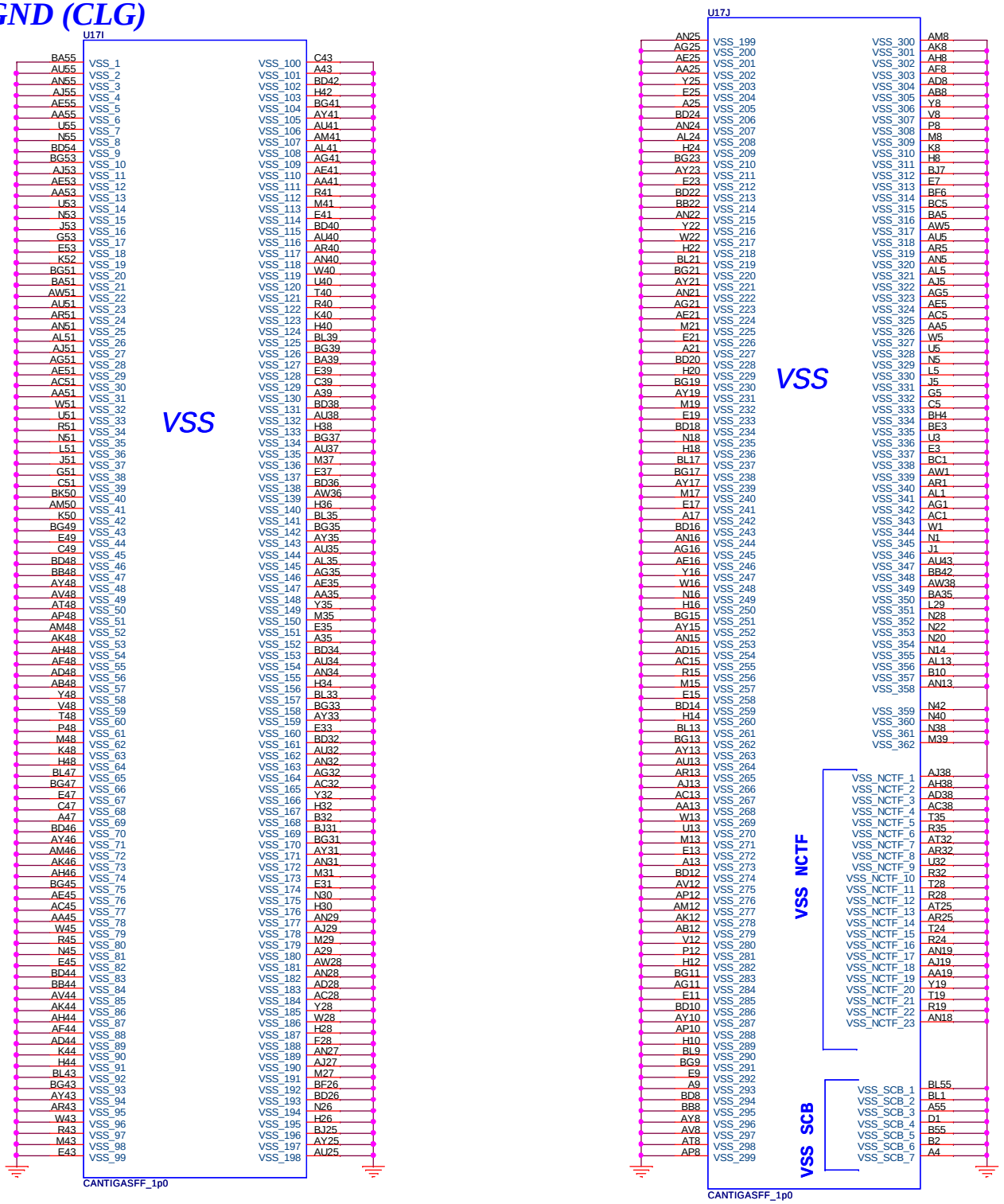
Cantiga SFF - GND (CLG)



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Title	Cantiga SFF (GND)
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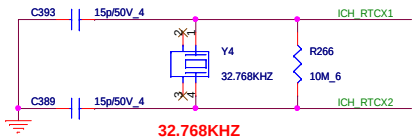
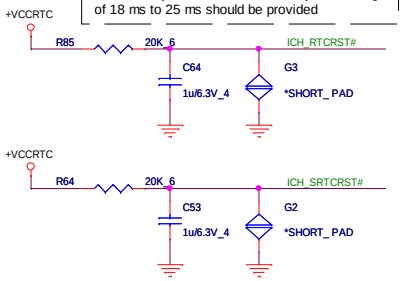
RTC CRYSTAL

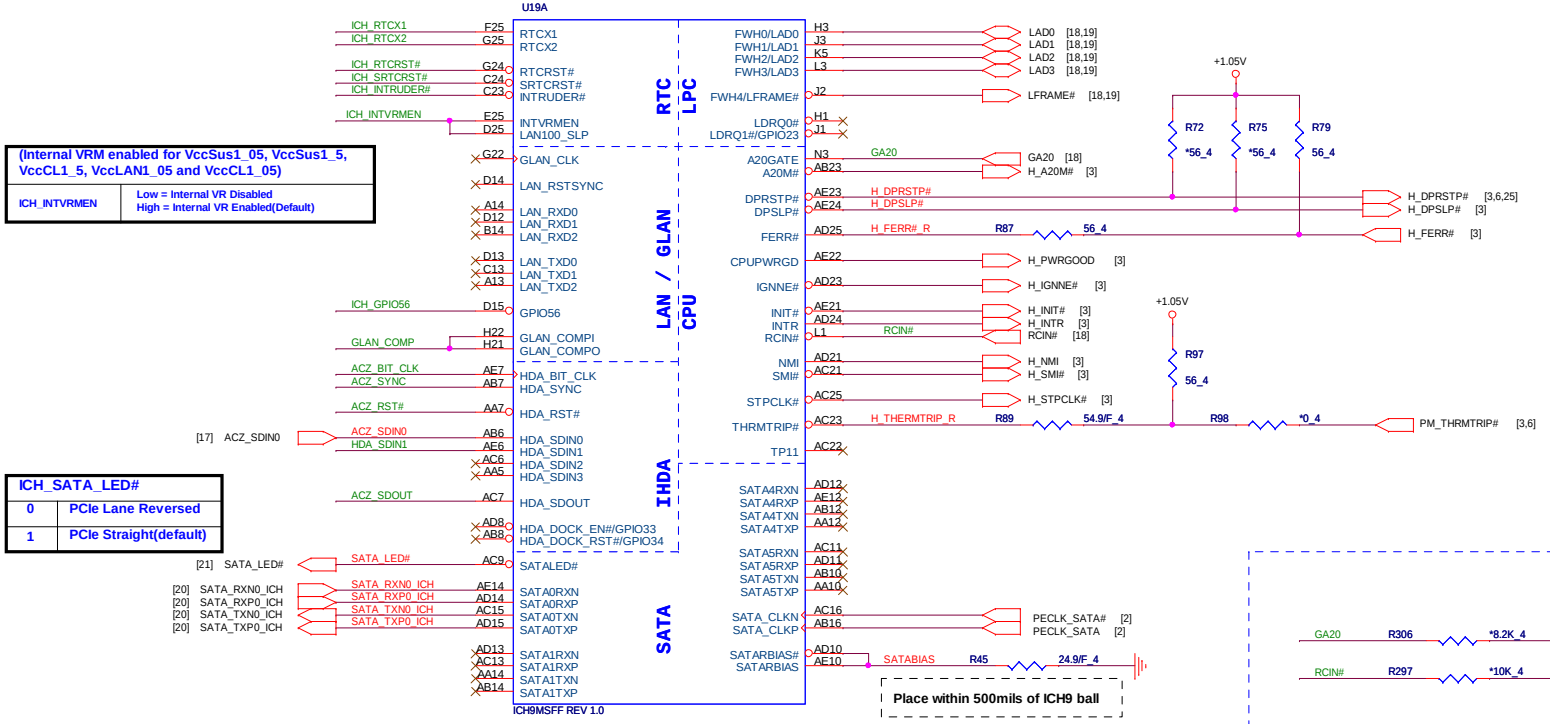


RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided



ICH9M SFF - Host,SATA,HDA (CLG)

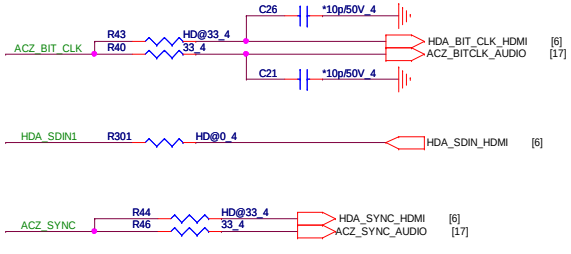


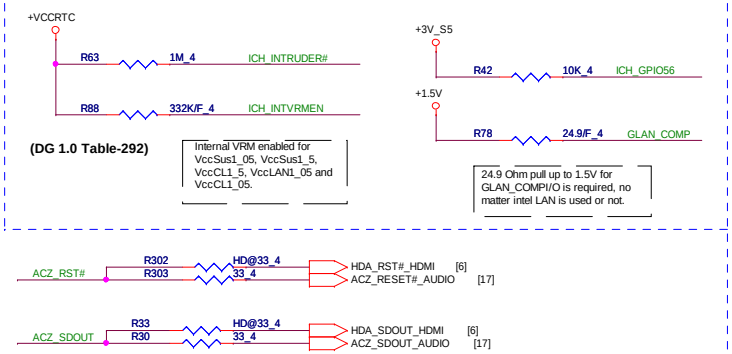
(Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

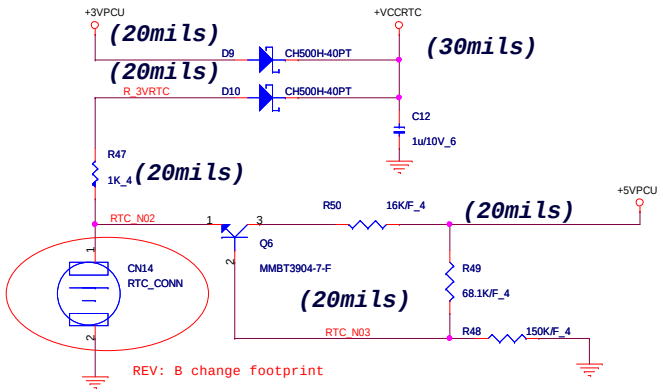
ICH_SATA_LED#	
0	PCIe Lane Reversed
1	PCIe Straight(default)

HD Audio Interface





RTC BATTERY (RTC)



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT / Description 0 / 0 / RSVD	REV: B del. R282 , add T23
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	0 / 1 / Enter XOR Chain 1 / 0 / Normal opration(Default) 1 / 1 / Set PCIE port config bit 1	ACZ_SDOUT T24, ACZ_SYNC T25 REV: B del. R36 & R39 , add T24 & T25

Title	ICH9M SFF (Host/SATA/HDA)		
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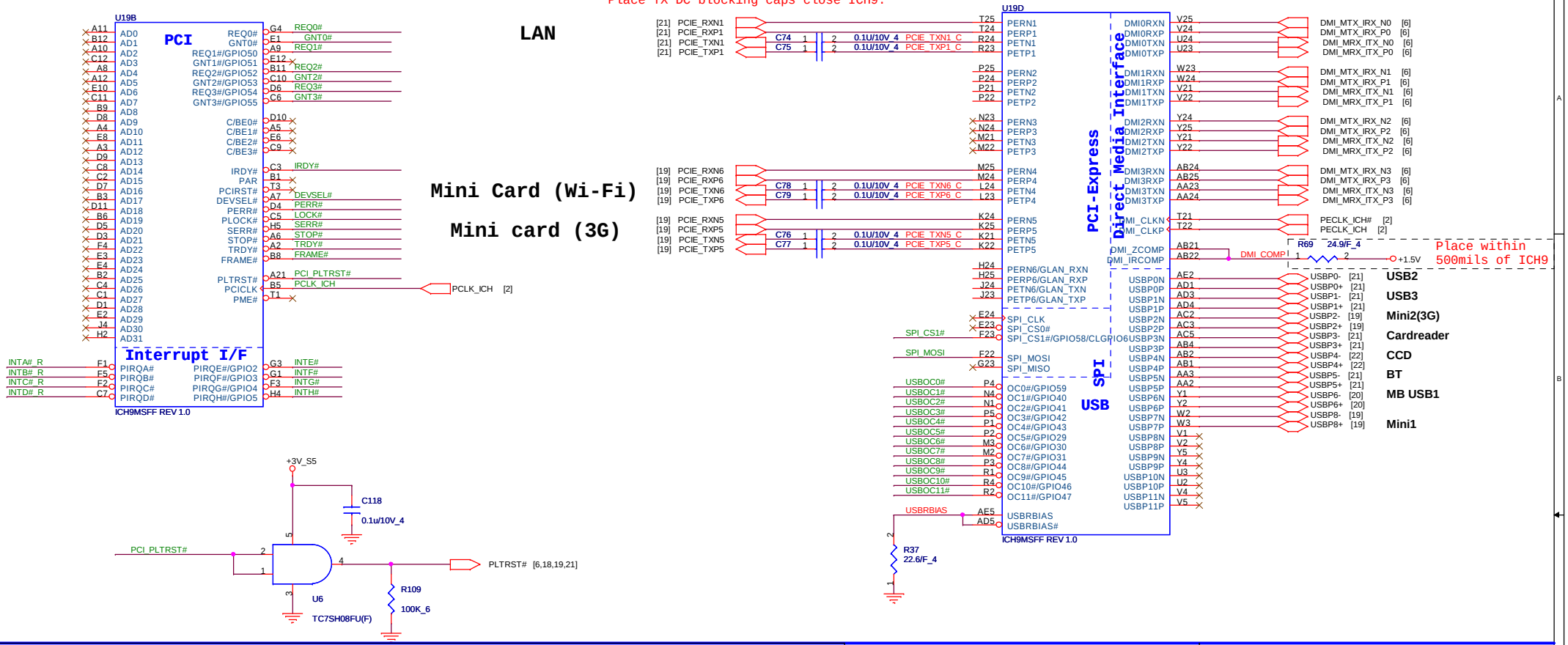
ICH9M SFF - USB/PCIE/DMI (CLG)

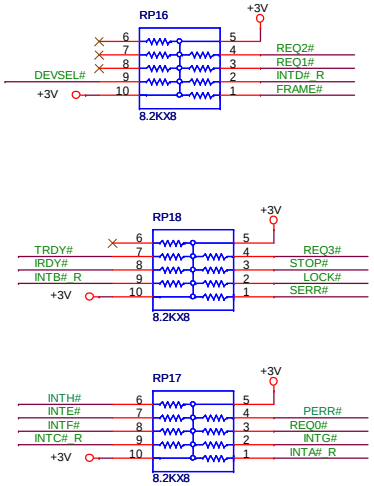


South Bridge Strap Pin (2/3)

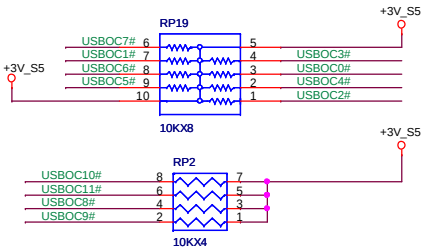
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	GNT2# — T6
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# — T4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI — T11
GNT0#	Boot BIOS Selection 0	PWROK		GNT0# — T2
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# — T10

PCI_GNT#0	SPI_CS#1	Boot Location
0	1	SPI(Default)
1	0	PCI

PCI PULL-UP



USBOC# PULL-UP



QUANTA COMPUTER

Title	ICH9M SFF (USB/PCIE/DMI)	
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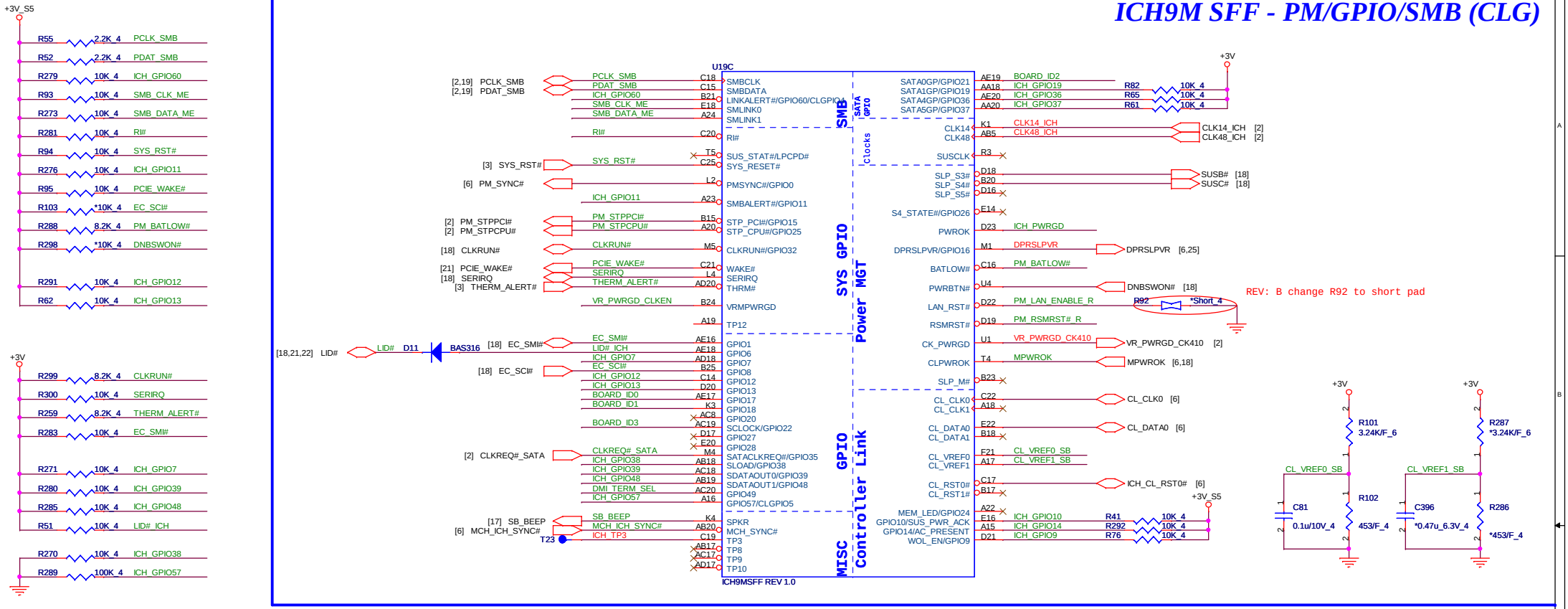
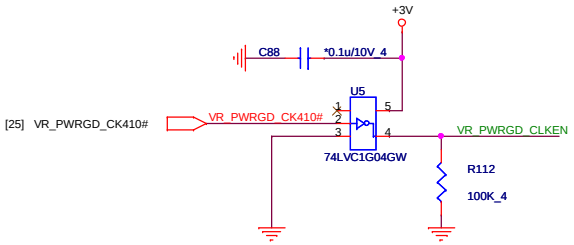
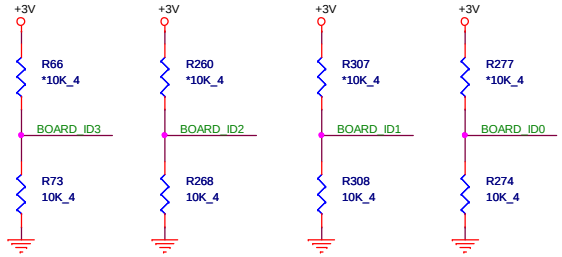
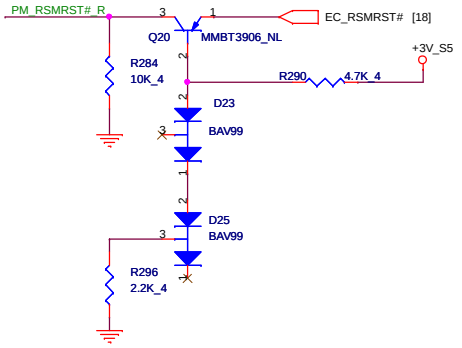
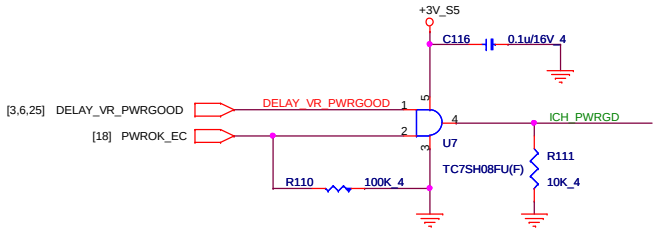
ICH9M SFF - PM/GPIO/SMB (CLG)











South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
PCBEEP	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL T12

QUANTA COMPUTER

Title	ICH9M SFF (PM/GPIO/SMB)	
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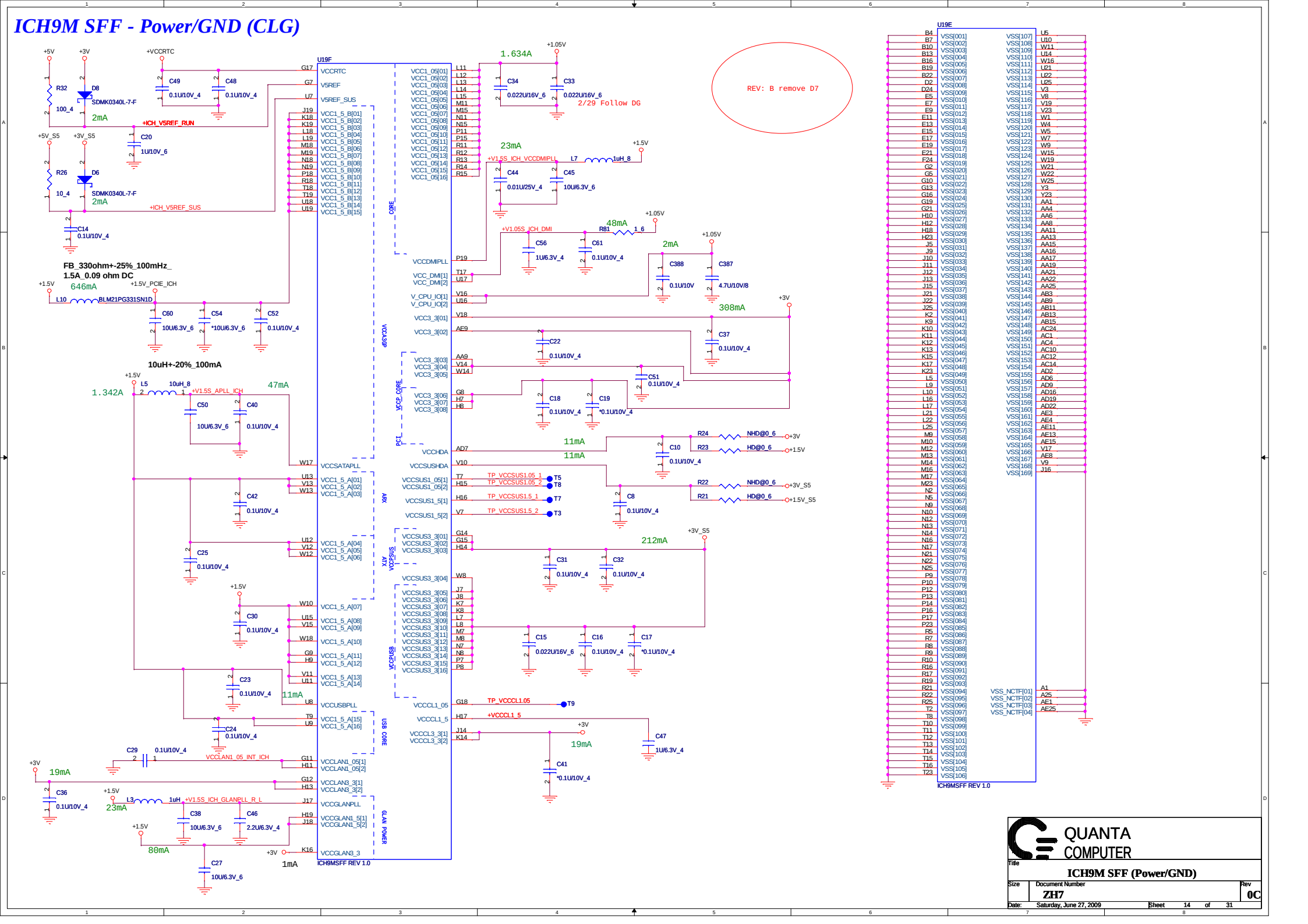
ICH9M SFF - Power/GND (CLG)



Title	ICH9M SFF (Power/GND)
Size	
Document Number	ZH7
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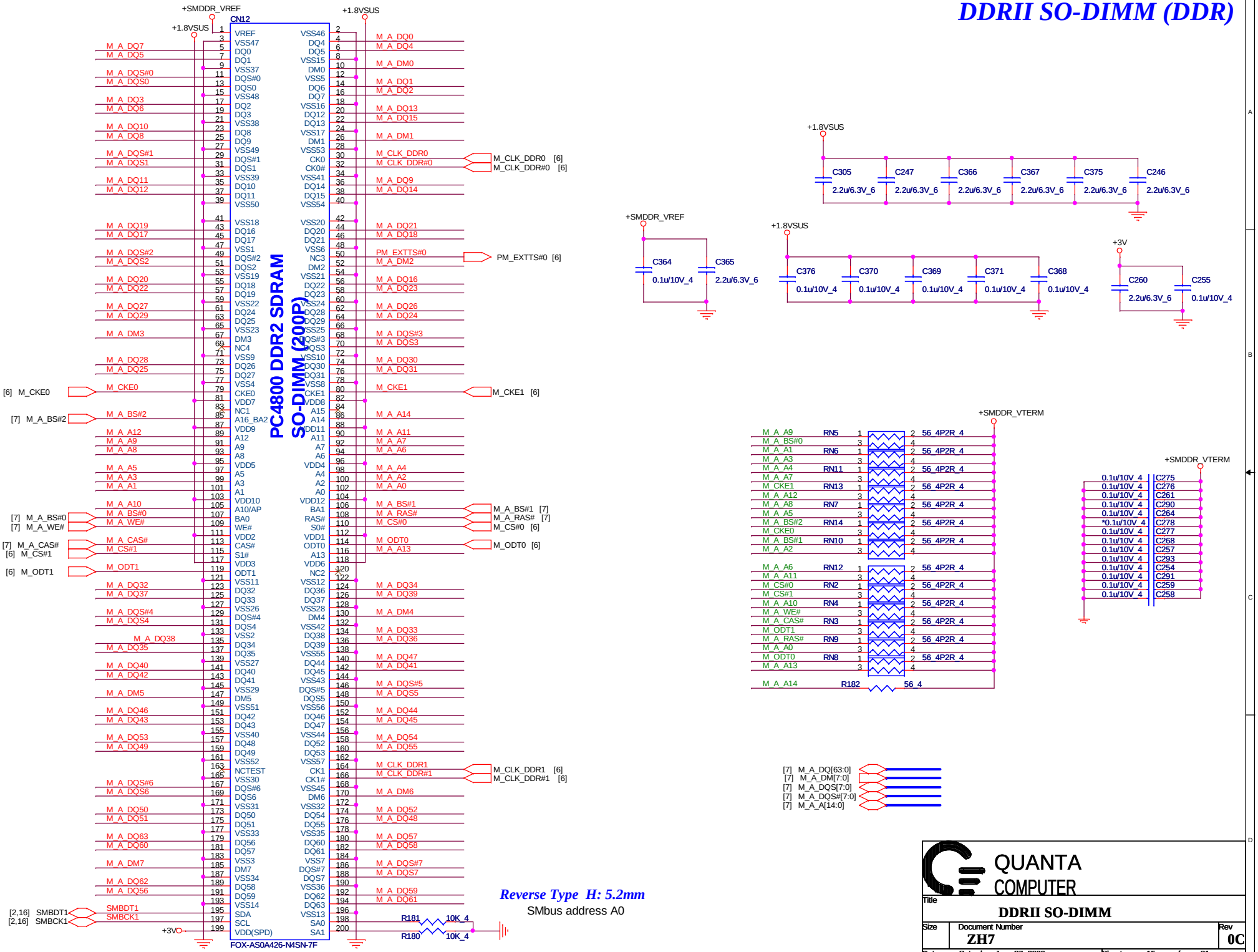
QUANTA COMPUTER

DDRII SO-DIMM (DDR)



Title	DDRII SO-DIMM	
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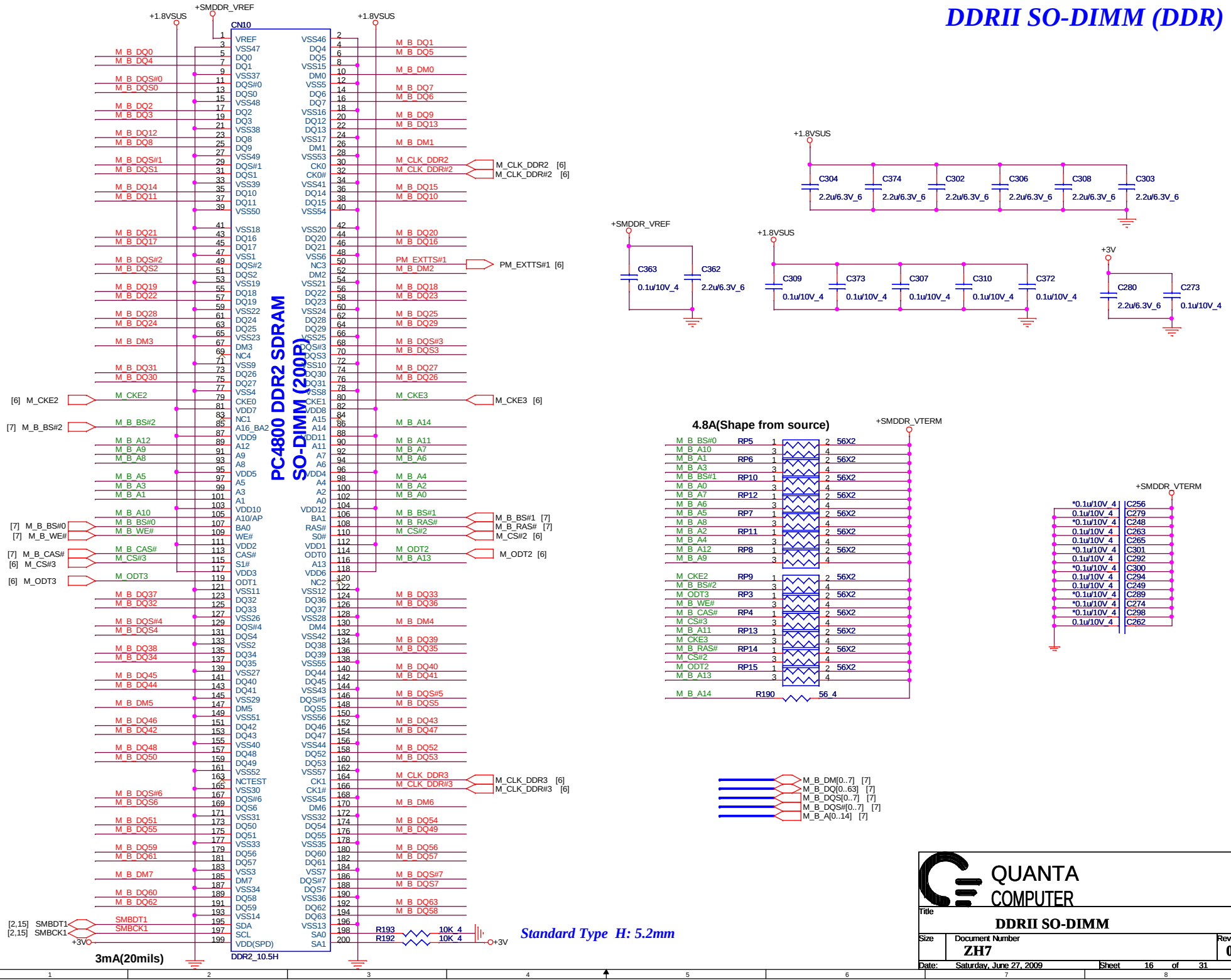
QUANTA COMPUTER

DDRII SO-DIMM (DDR)



Standard Type H: 5.2mm

Title	DDRII SO-DIMM	
Size	Document Number ZH7	Rev 0C
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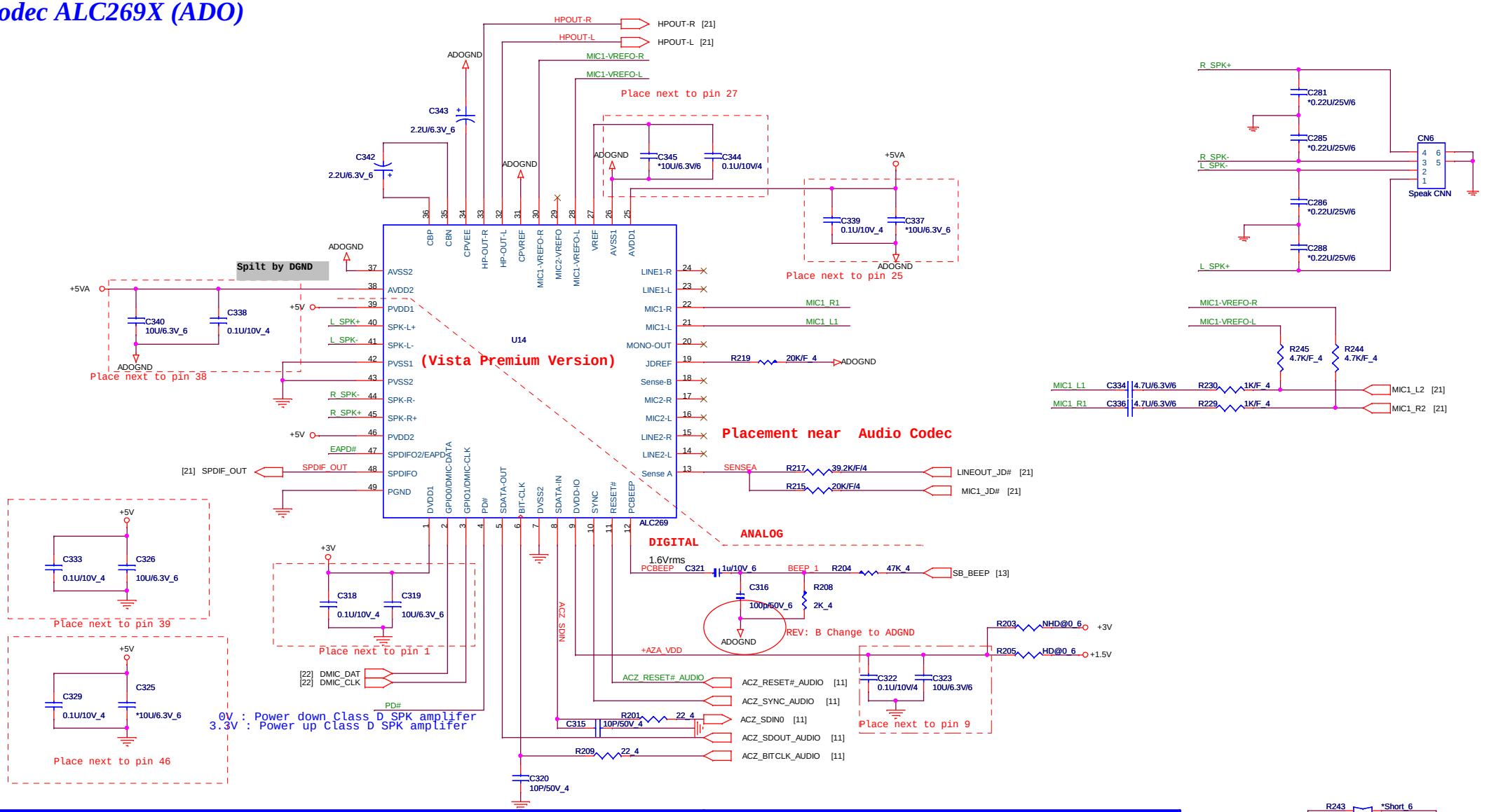
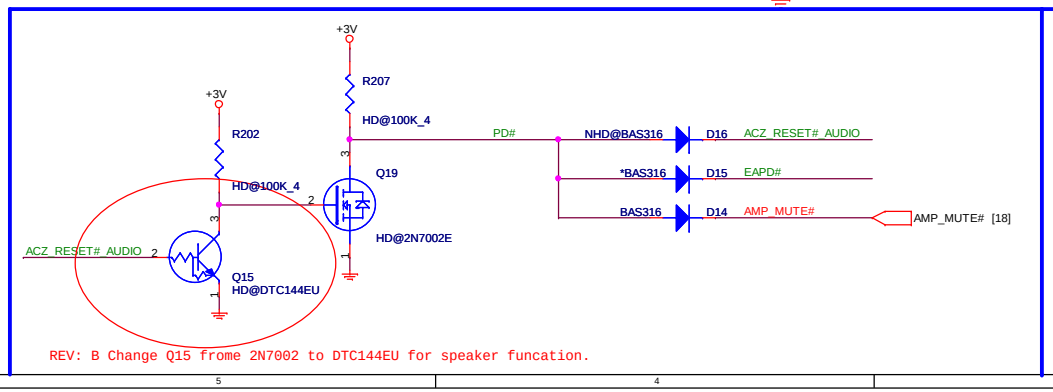
QUANTA COMPUTER

Codec ALC269X (ADO)

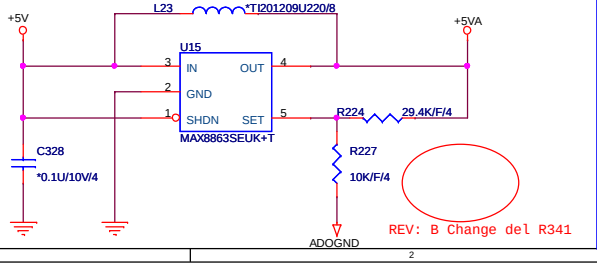


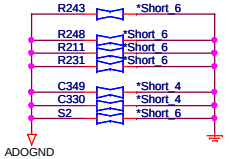


Power (ADO)

Demodulation Filter

Place close to Codec





QUANTA COMPUTER

Title	Codec ALC269X	
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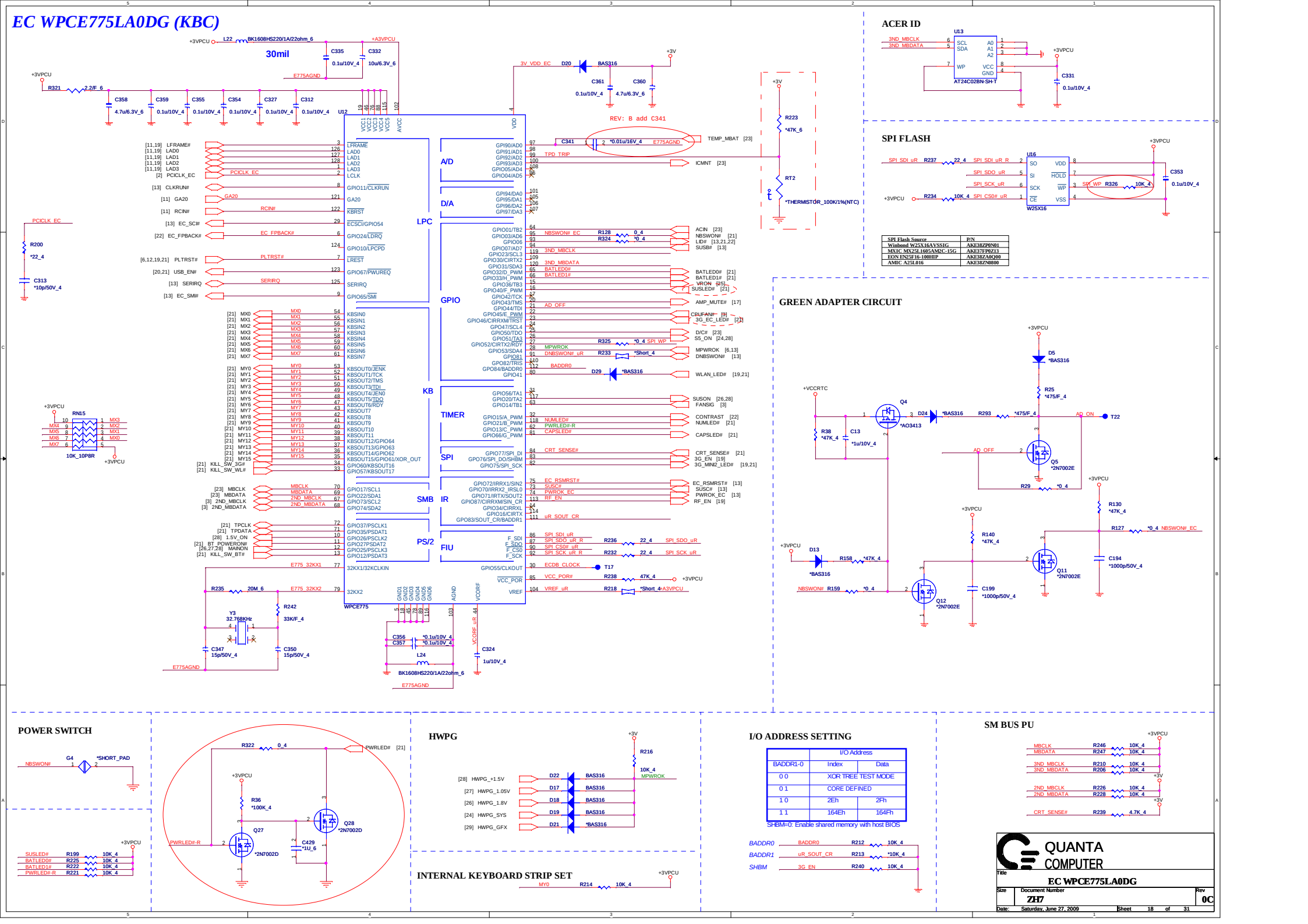
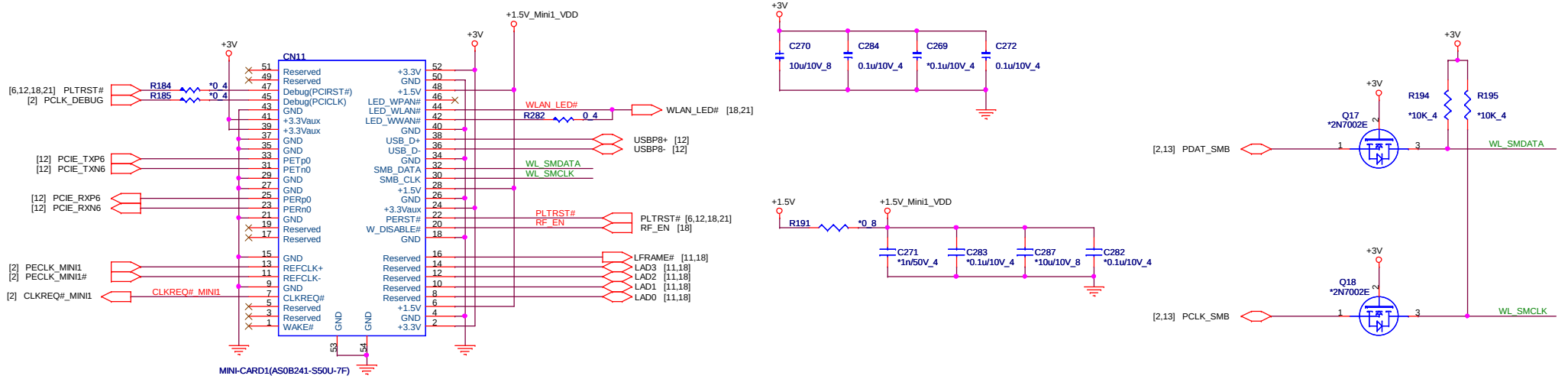
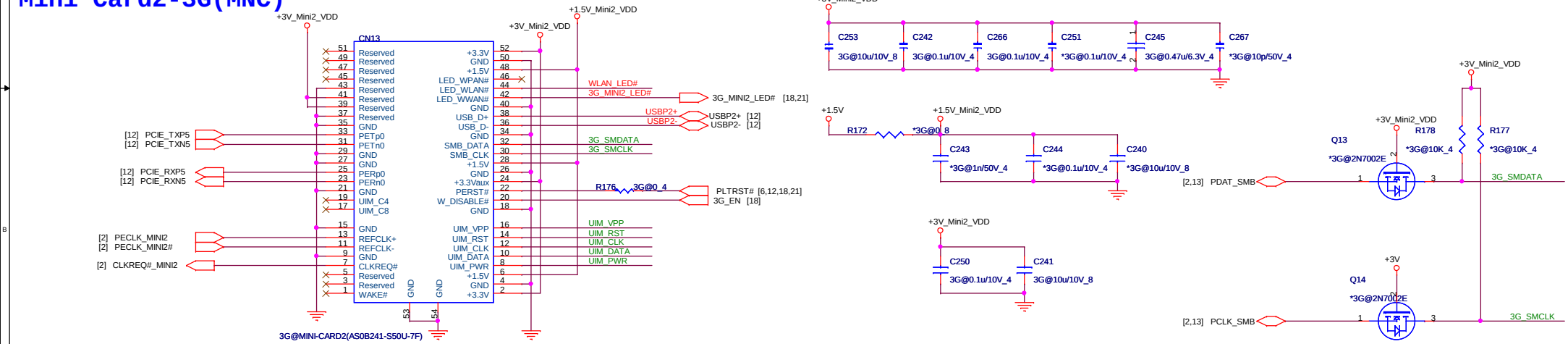
EC WPCE775LA0DG (KBC)

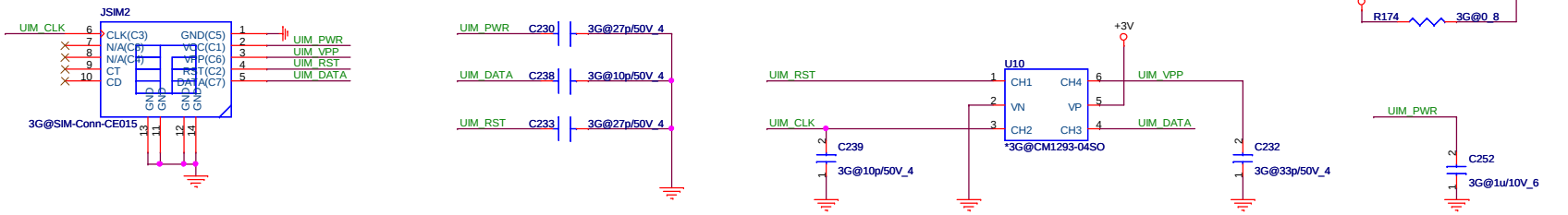


Mini Card1-WLAN/WMAX(MPC)



Mini Card2-3G(MNC)





QUANTA COMPUTER		
Title: MINI PCIE (WLAN/WMAX/3G)		
Size	Document Number: ZH7	Rev: 0C
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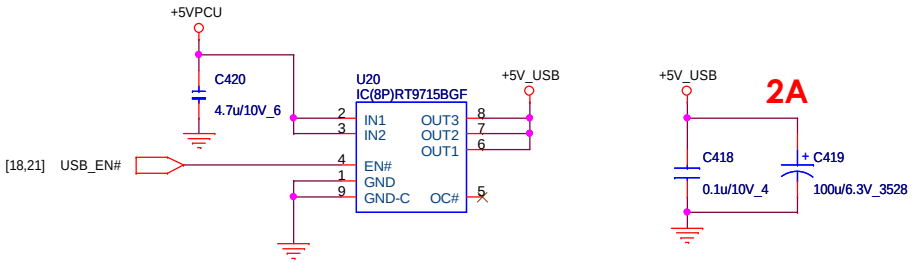
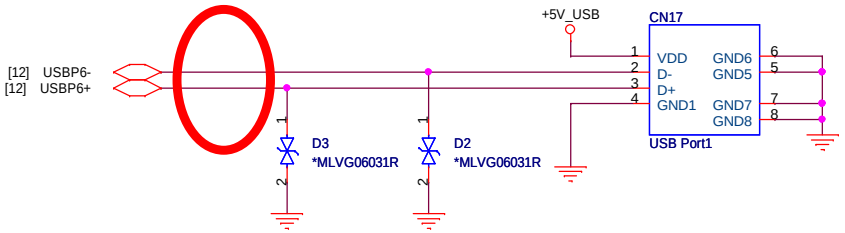
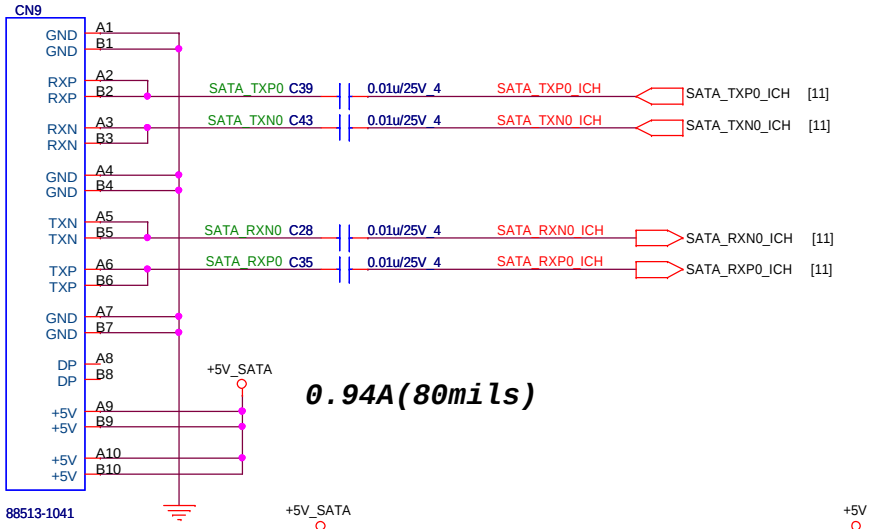
MB USB (USB)



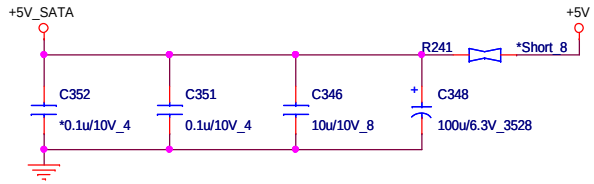
Remove R6、R7、L2



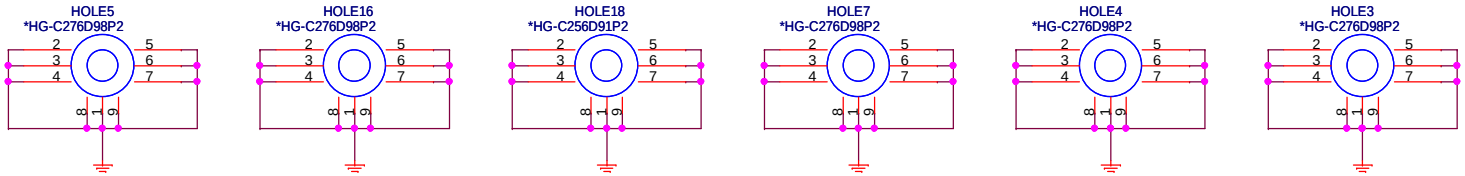
2.5" SATA HDD(HDD)

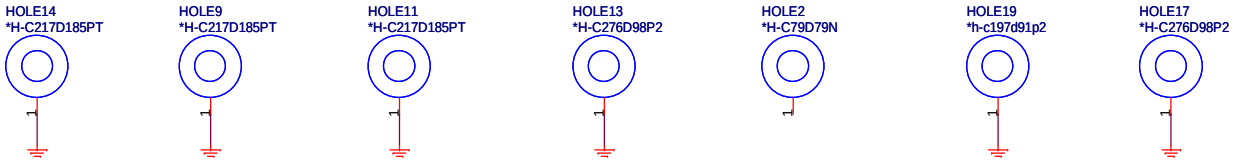


0.94A(80mils)

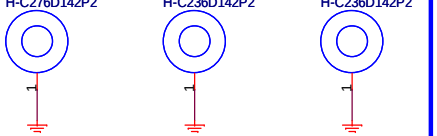


HOLE (EXC)

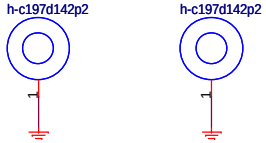


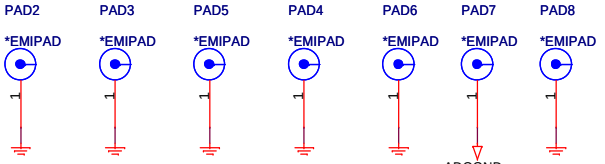


FAN nut



Minipci nut





QUANTA COMPUTER

Title	USB/HDD/HOLE	
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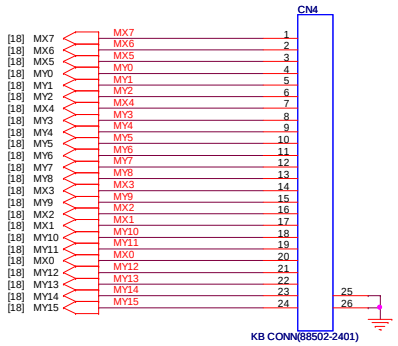
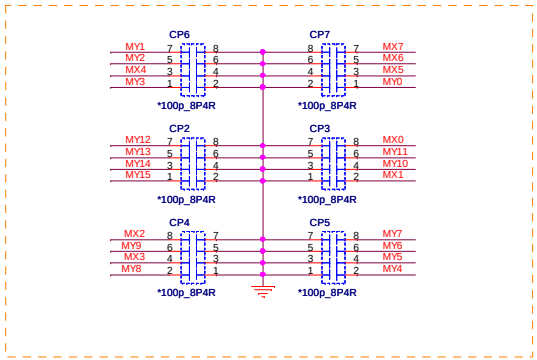
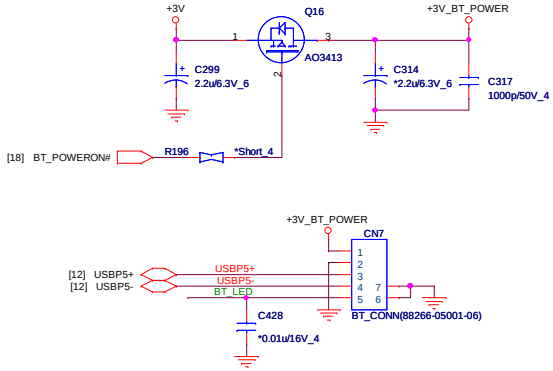
Keyboard(KBC)



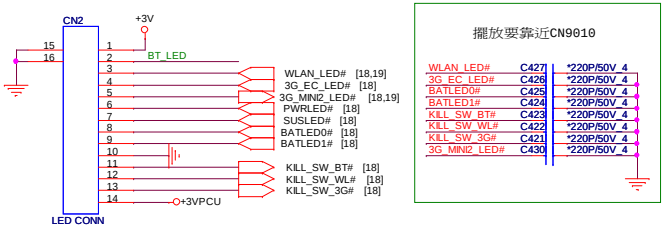
For EMI Reserve Caps for debug



BuleTooth (BTM)

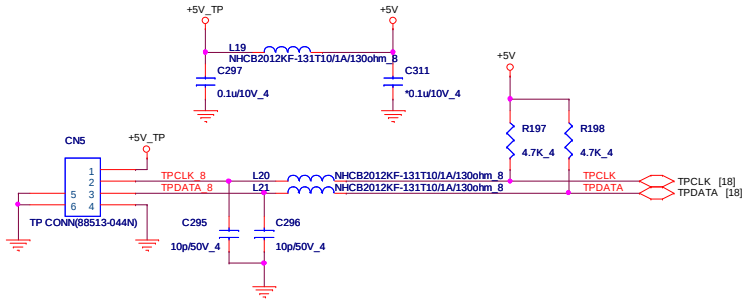


LED D/B (UIF)

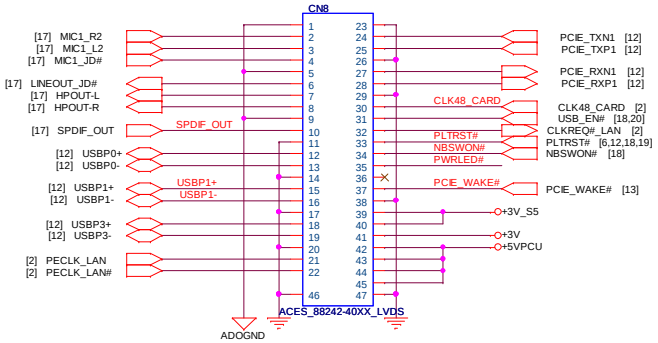


Check P/N footprint

Touch Pad D/B (TPD)

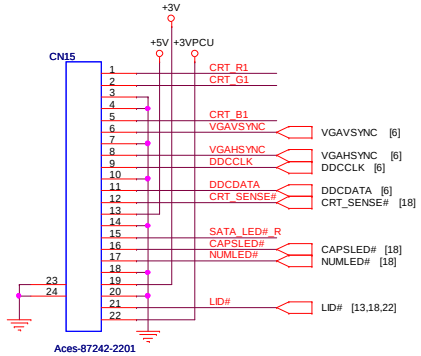


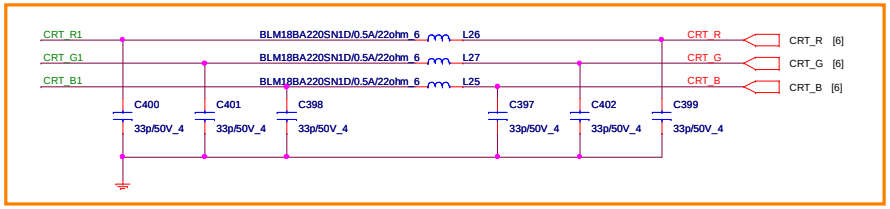
Card Reader/USB DB CONNECTER(MMC)/Power Connector



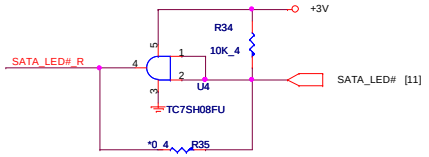
REV: B DEL CN8.36 SUSLED#

CRT D/B (UIF)





For EMI



QUANTA COMPUTER

Title	KB/BT/PR/TP/LAN/LED/CR Connects	
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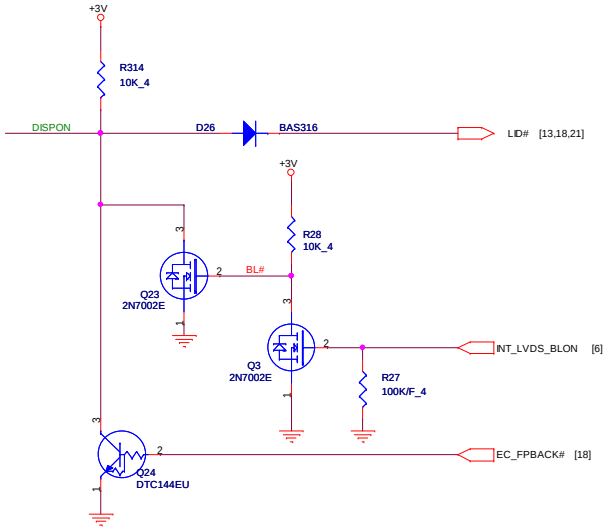
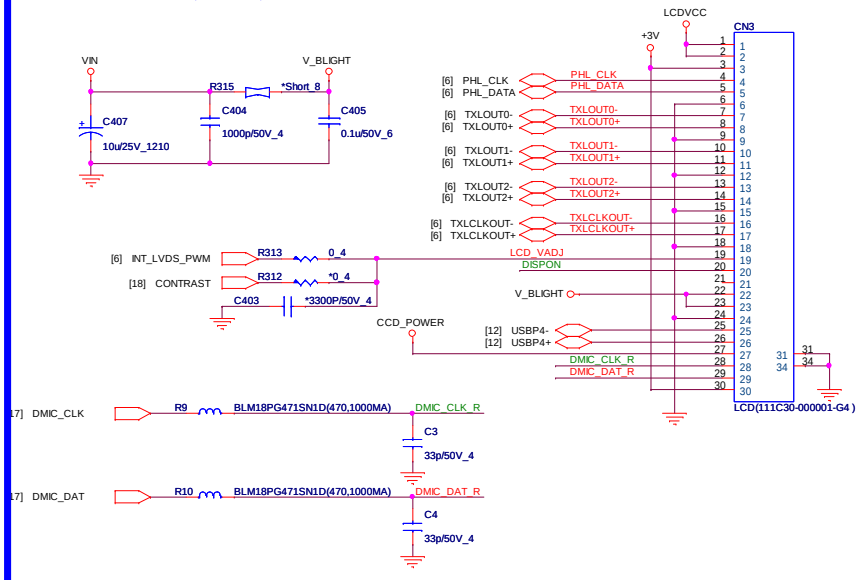
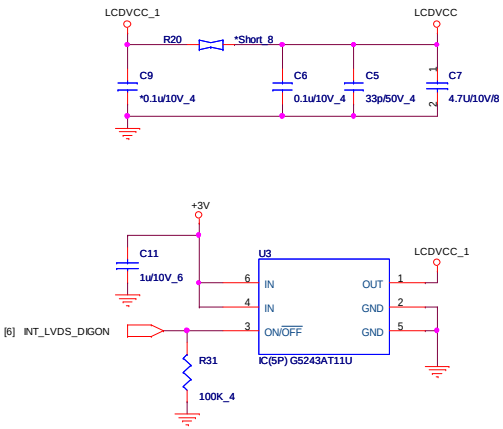
Backlight Control(LDS)



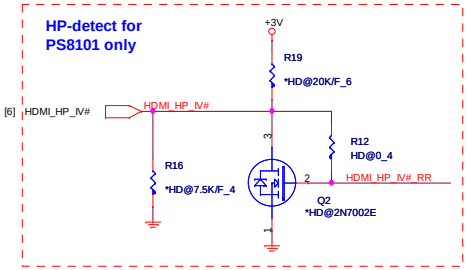
LED Panel(LDS)

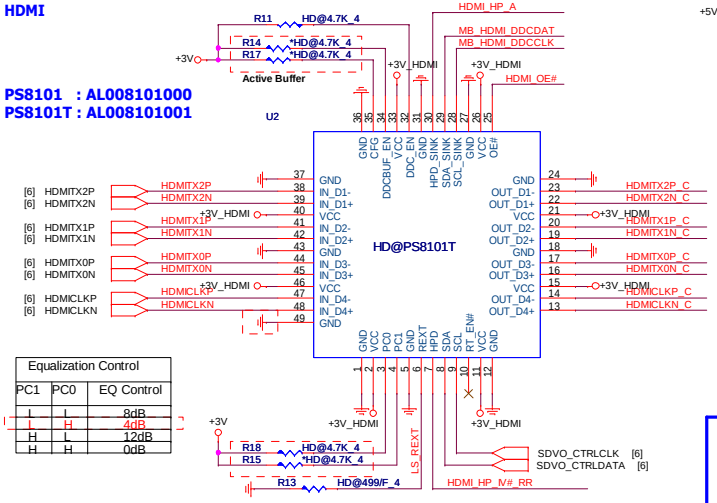


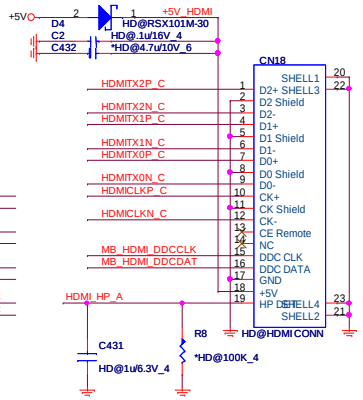
LED Panel POWER SWITCH(LDS)



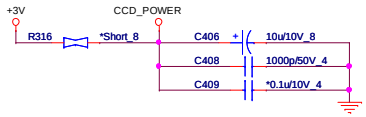
HDMI(HDM)



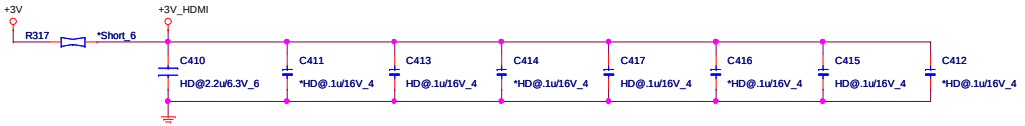




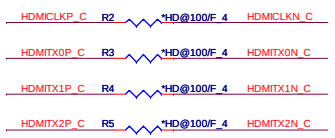
Camera(CCD)

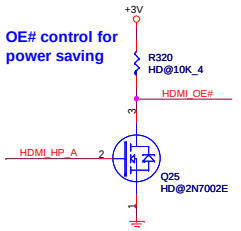


SDVO I2C Control



FOR EMI





QUANTA COMPUTER

Title	LED Panel/CCD/HDMI	
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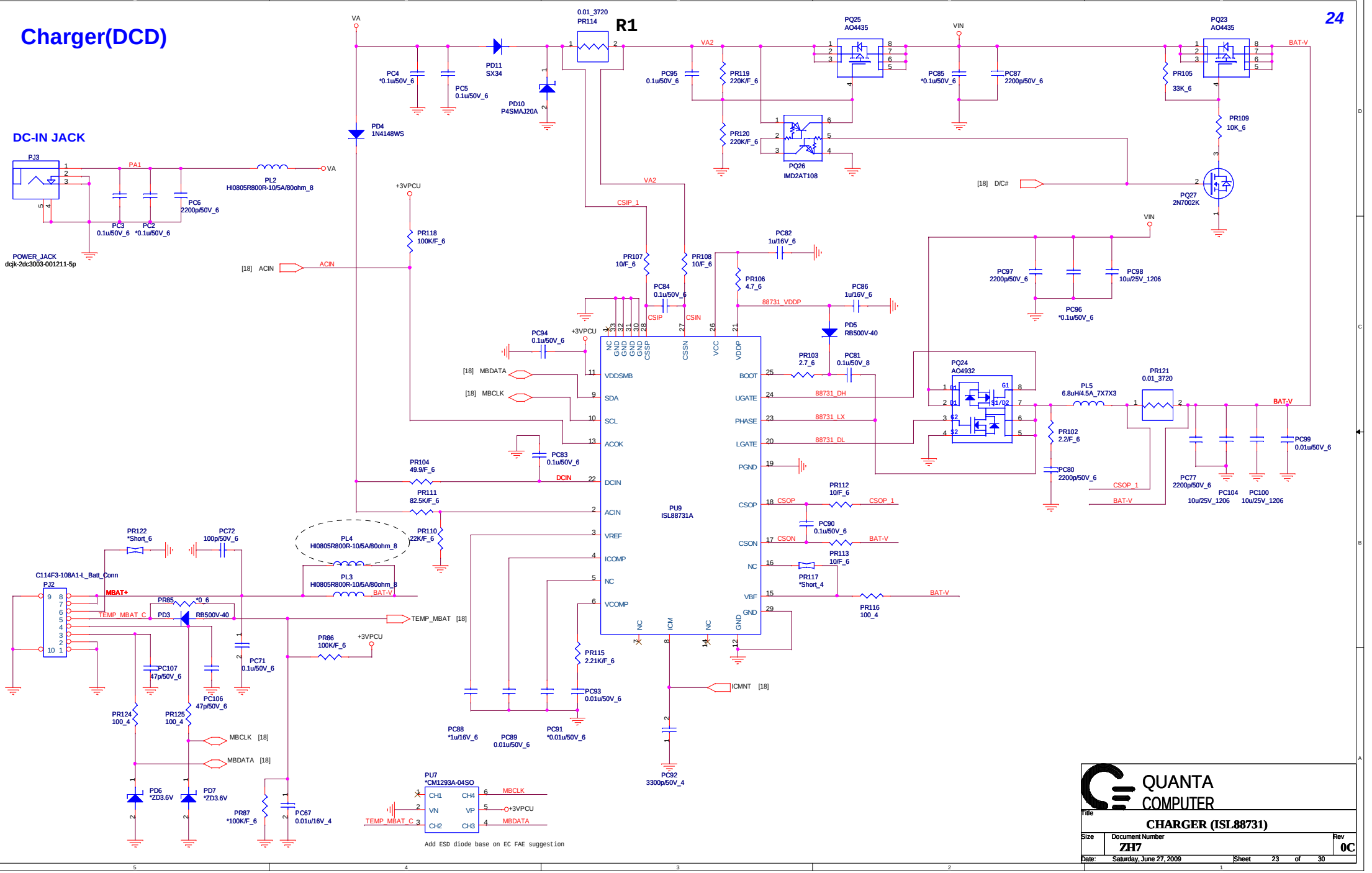
Charger(DCD)

DC-IN JACK



Title	CHARGER (ISL88731)	
Size	Document Number: ZH7	Rev: 0C
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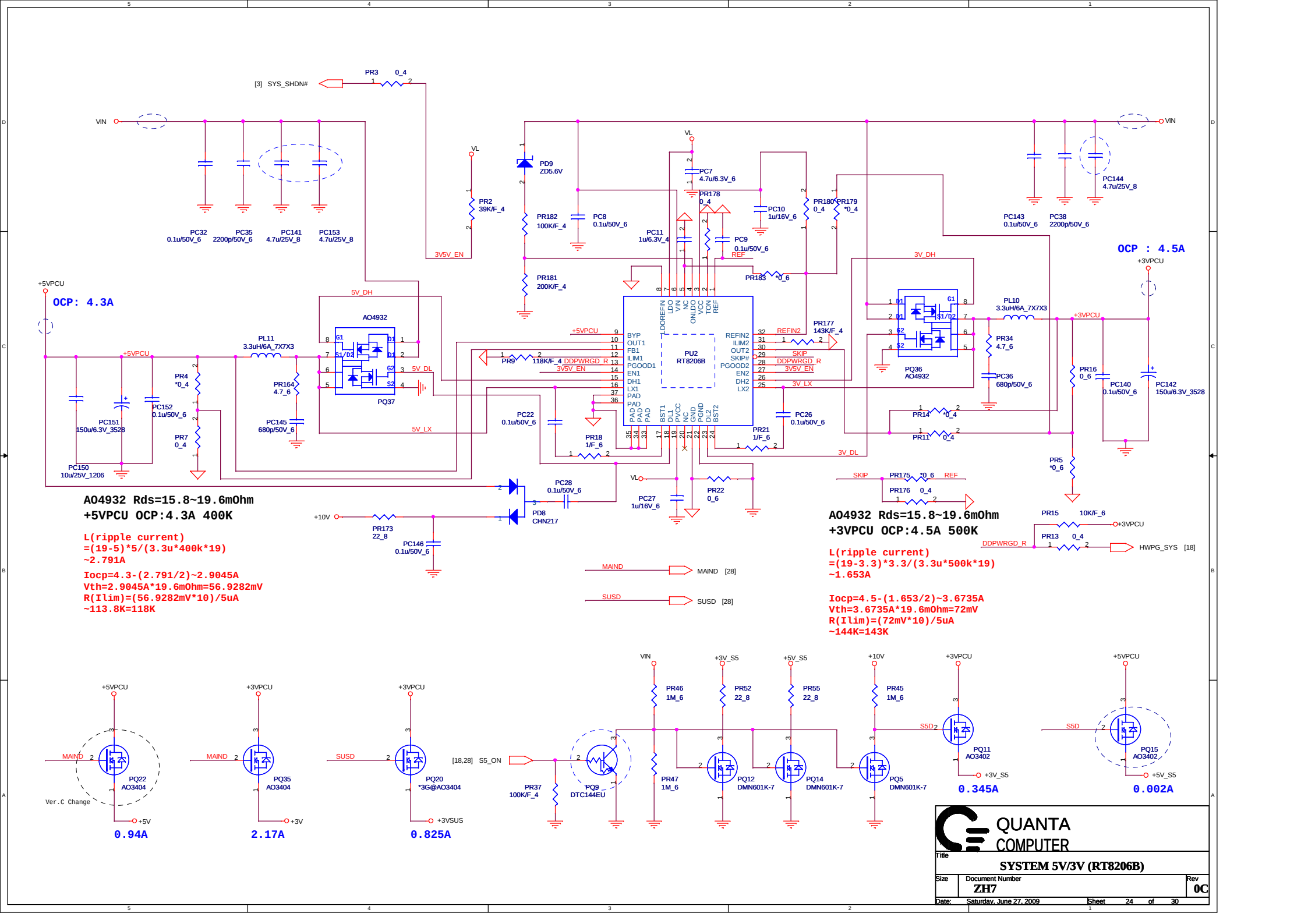
[3] SYS_SHDN#
PR3 0_4
VIN
PC32 0.1u/50V_6
PC35 2200p/50V_6
PC141 4.7u/25V_8
PC153 4.7u/25V_8
VL
PR2 39K/F_4
3V5V_EN
PD9 ZD5.6V
PR182 100K/F_4
PR181 200K/F_4
PC8 0.1u/50V_6
PC7 4.7u/6.3V_6
PR178 0_4
PC10 1u/16V_6
PR180 0_4
PR179 *0_4
PC11 1u/6.3V_4
PC9 0.1u/50V_6
REF
PR183 *0_6
PC144 4.7u/25V_8
PC143 0.1u/50V_6
PC38 2200p/50V_6
OCP : 4.5A
+3VPCU
3V_DH
+5VPCU
OCP: 4.3A
5V_DH
AO4932
PL11 3.3uH/6A_7X7X3
PR4 *0_4
PR7 0_4
PC151 150u/6.3V_3528
PC152 0.1u/50V_6
PC150 10u/25V_1206
PR164 4.7_6
PC145 680p/50V_6
PQ37
5V_DL
5V_LX
PR9 118K/F_4
DDPWRGD_R
3V5V_EN
PU2 RT8206B
DOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD
PAD PAD PAD BST1 DL1 PVCC NC GND PGND DL2 BST2
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
PC22 0.1u/50V_6
PR18 1/F_6
PC28 0.1u/50V_6
PD8 CHN217
PR173 22_8
PC146 0.1u/50V_6
+10V
PC27 1u/16V_6
PR22 0_6
PC26 0.1u/50V_6
PR21 1/F_6
3V_LX
3V_DL
REFIN2
PR177 143K/F_4
SKIP
PQ36 AO4932
PL10 3.3uH/6A_7X7X3
PR34 4.7_6
PC36 680p/50V_6
PR14 *0_4
PR11 0_4
PR16 0_6
PC140 0.1u/50V_6
PC142 150u/6.3V_3528
PR5 *0_6
SKIP
PR175 *0_6
REF
PR176 0_4
PR15 10K/F_6
PR13 0_4
HWPG_SYS [18]
MAIND
MAIND [28]
SUSD
SUSD [28]
AO4932 Rds=15.8~19.6mOhm
+5VPCU OCP:4.3A 400K
L(ripple current)
=(19-5)*5/(3.3u*400k*19)
~2.791A
Iocp=4.3-(2.791/2)~2.9045A
Vth=2.9045A*19.6mOhm=56.9282mV
R(Ilim)=(56.9282mV*10)/5uA
~113.8K=118K
AO4932 Rds=15.8~19.6mOhm
+3VPCU OCP:4.5A 500K
L(ripple current)
=(19-3.3)*3.3/(3.3u*500k*19)
~1.653A
Iocp=4.5-(1.653/2)~3.6735A
Vth=3.6735A*19.6mOhm=72mV
R(Ilim)=(72mV*10)/5uA
~144K=143K
PQ22 AO3404
Ver.C Change
+5V
0.94A
PQ35 AO3404
+3V
2.17A
PQ20 *3G@AO3404
+3VSUS
0.825A
[18,28] S5_ON
PR37 100K/F_4
PQ9 DTC144EU
PR46 1M_6
PR47 1M_6
+3V_S5
PR52 22_8
PQ12 DMN601K-7
+5V_S5
PR55 22_8
PQ14 DMN601K-7
PR45 1M_6
PQ5 DMN601K-7
SSD
PQ11 AO3402
0.345A
PQ15 AO3402
0.002A
QUANTA COMPUTER
Title
SYSTEM 5V/3V (RT8206B)
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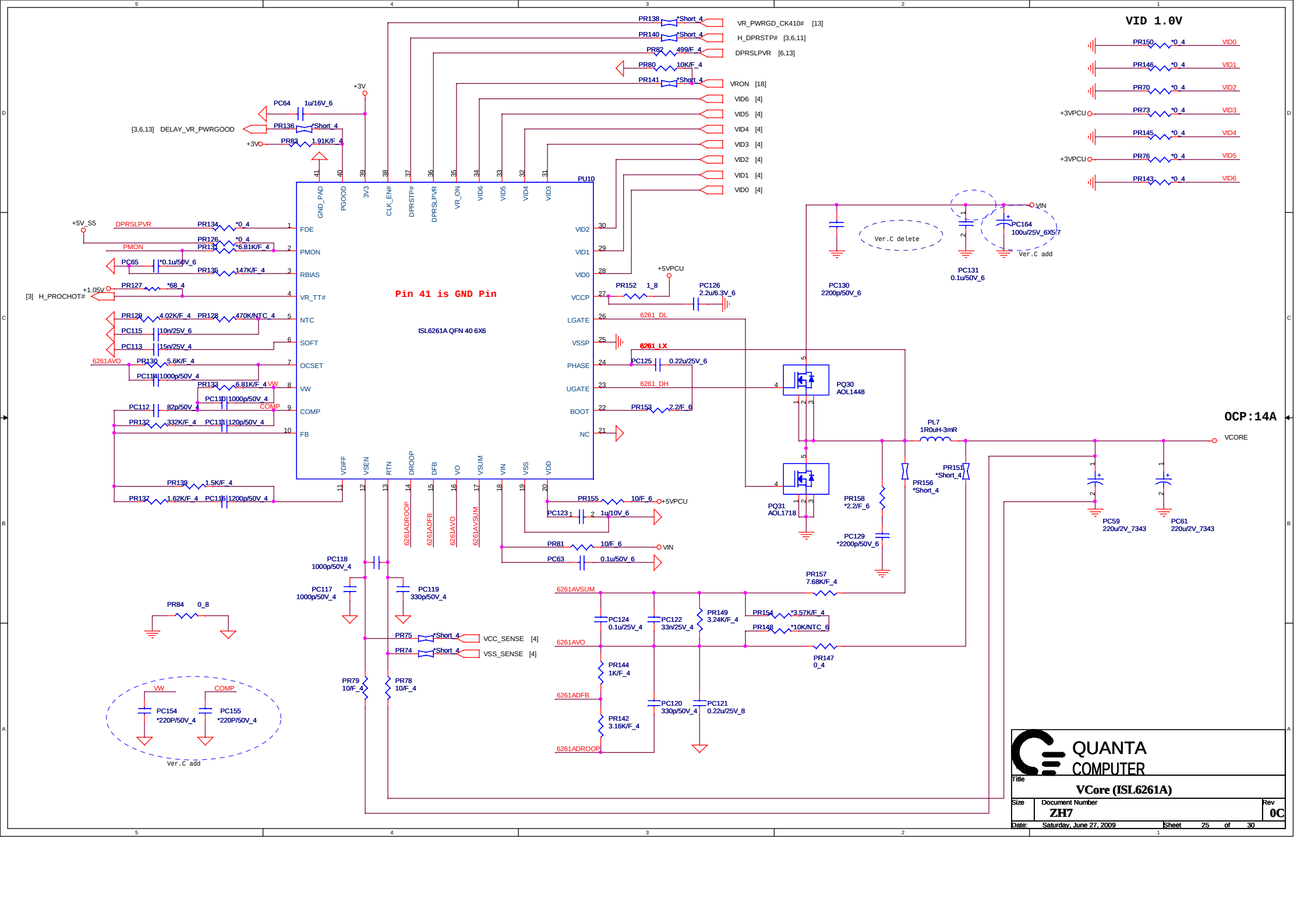
VID 1.0V
OCP:14A
Pin 41 is GND Pin
ISL6261A QFN 40 6X6
PU10
GND_PAD
PGOOD
3V3
CLK_EN#
DPRSTP#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
FDE
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
VID2
VID1
VID0
VCCP
LGATE
VSSP
PHASE
UGATE
BOOT
NC
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
VSS
VDD
VCORE
VIN
+5VPCU
+3V
+5V_S5
+1.05V
PQ30 AOL1448
PQ31 AOL1718
PL7 1R0uH-3mR
PC59 220u/2V_7343
PC61 220u/2V_7343
PC164 100u/25V_6X5.7
Ver.C delete
Ver.C add
VCC_SENSE [4]
VSS_SENSE [4]
VRON [18]
VR_PWRGD_CK410# [13]
H_DPRSTP# [3,6,11]
DPRSLPVR [6,13]
DELAY_VR_PWRGOOD [3,6,13]
H_PROCHOT# [3]
6261AVO
6261ADFB
6261ADROOP
6261AVSUM
6261_DL
6261_DH
6261_LX
Title
VCore (ISL6261A)
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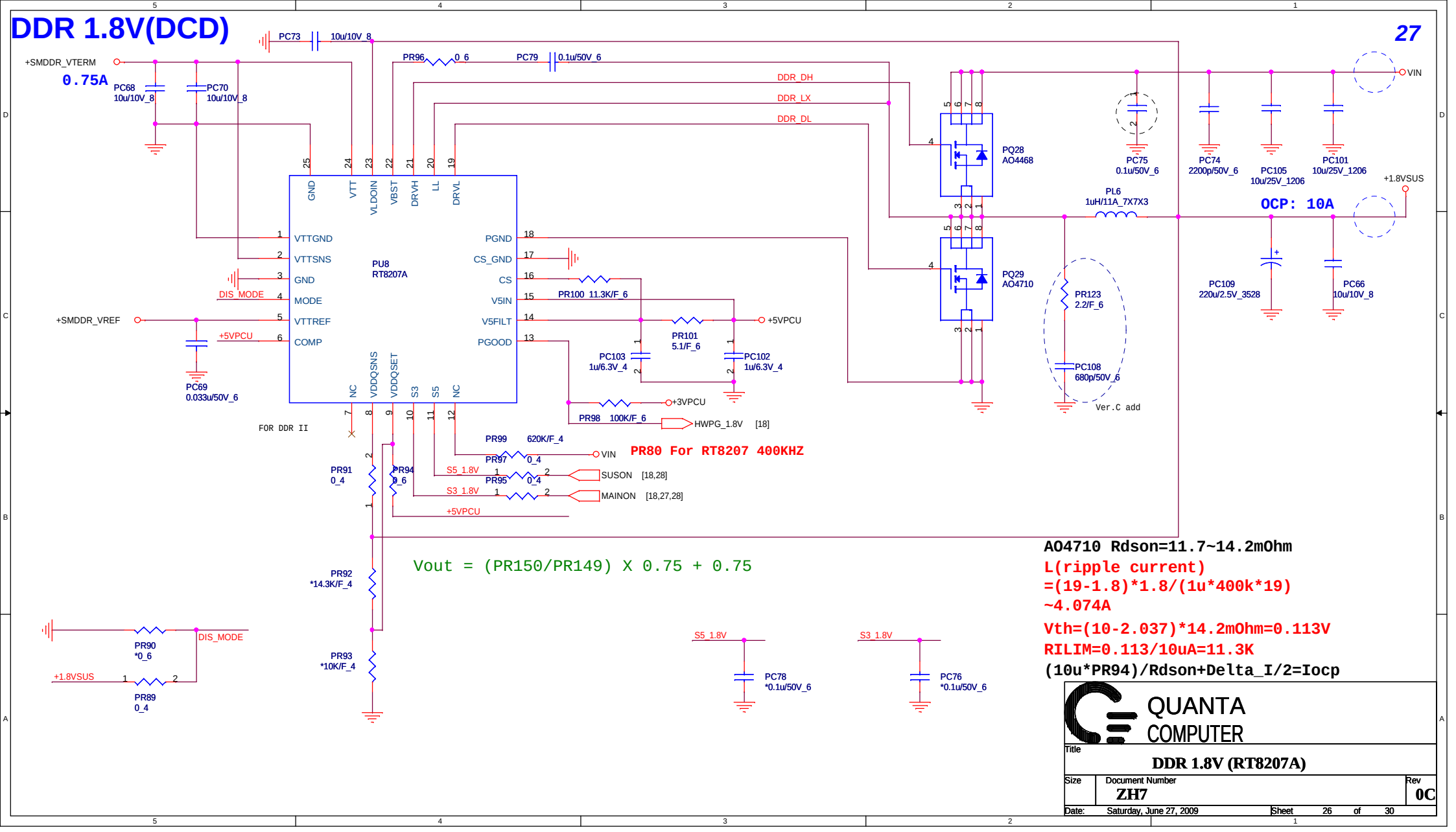
DDR 1.8V(DCD)



AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.8)*1.8/(1u*400k*19)
~4.074A

Vth=(10-2.037)*14.2mOhm=0.113V

RILIM=0.113/10uA=11.3K

(10u*PR94)/Rdson+Delta_I/2=Iocp

QUANTA COMPUTER

Title: DDR 1.8V (RT8207A)		
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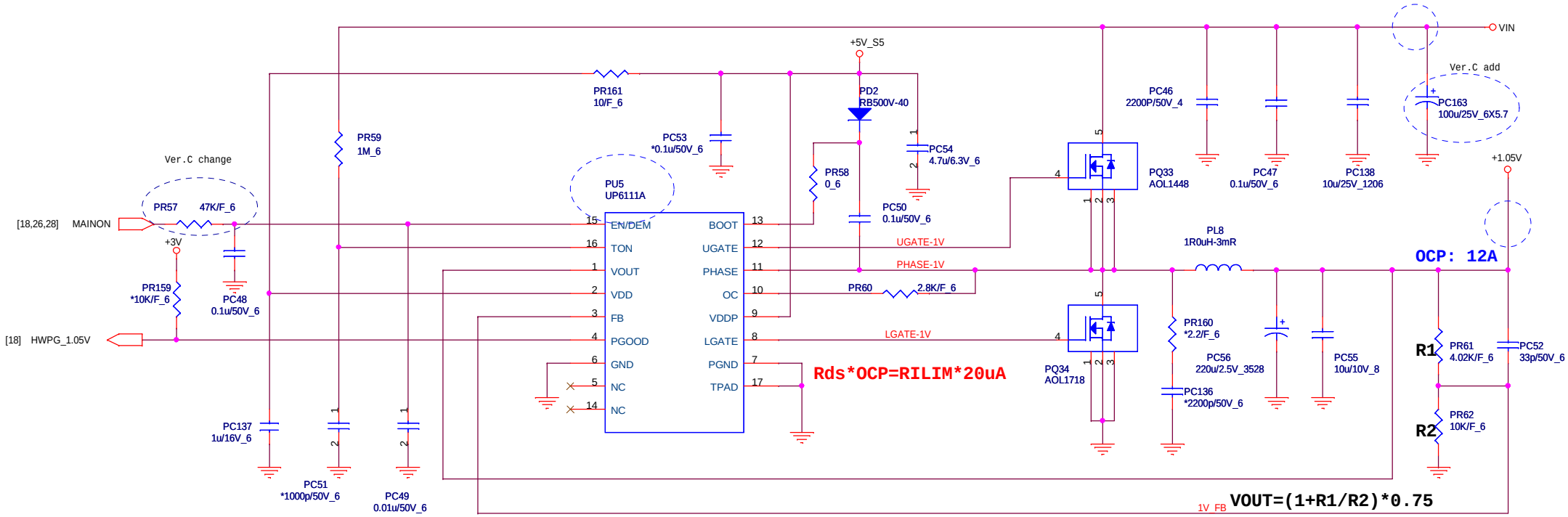


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

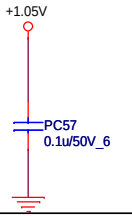
AOL1412 Rdson=4.6mOhm

OCP=16-0.8A

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

4.6m*12=RILIM*20uA

RILIM=2.76K--- 2.8K



QUANTA COMPUTER

Title: VCCP 1.05V (RT8202A)		
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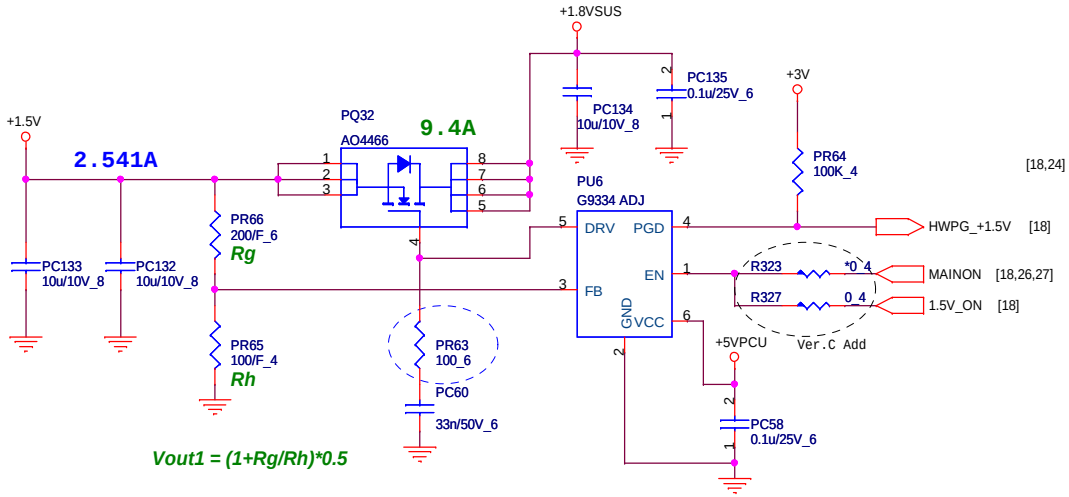
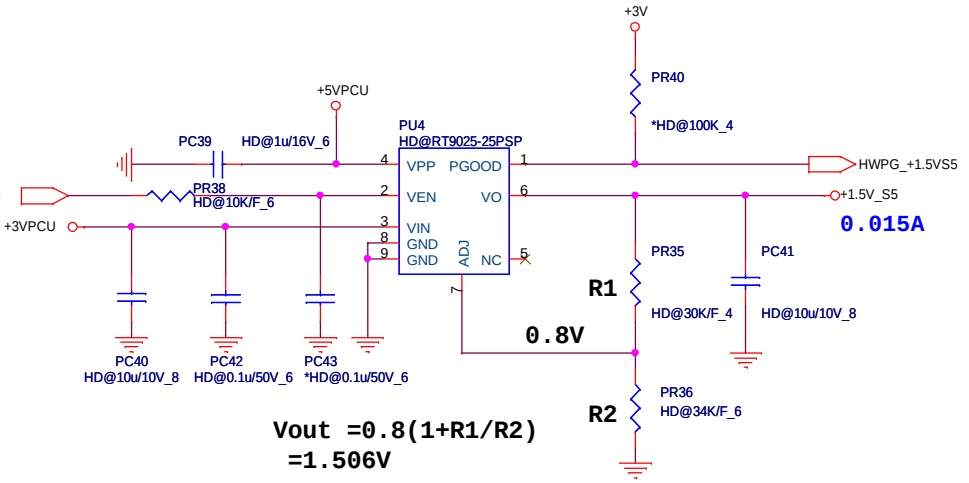
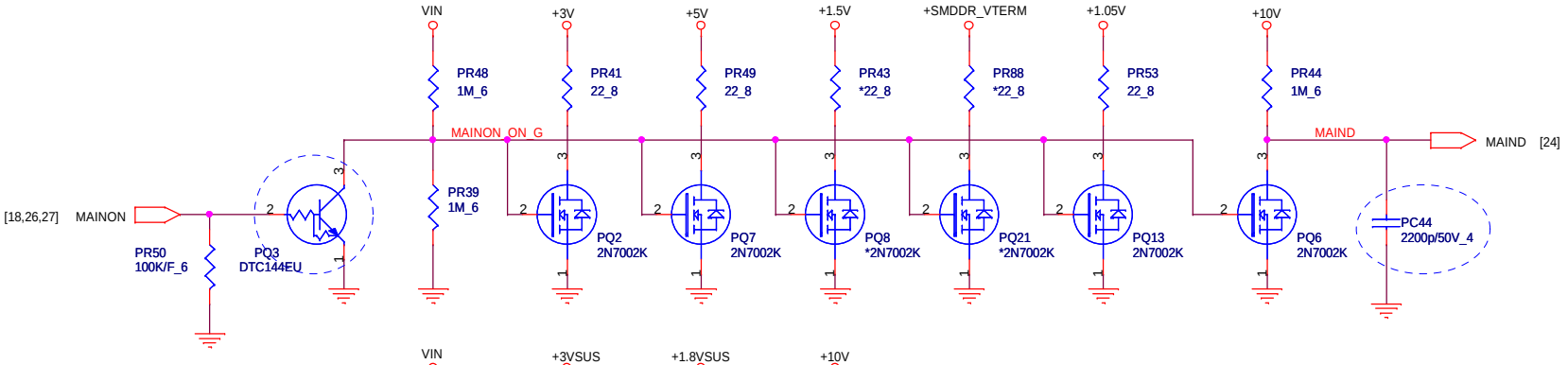
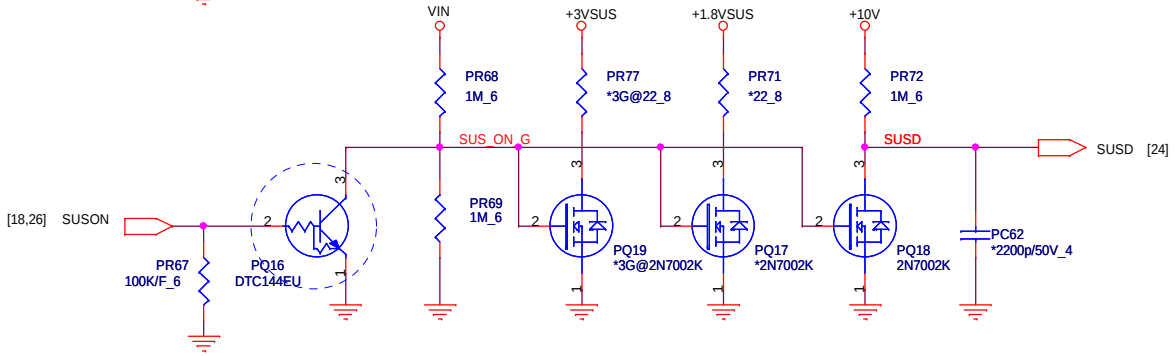
Discharger/1.5V(DCD)









QUANTA COMPUTER

Title: Discharge/1.5V		
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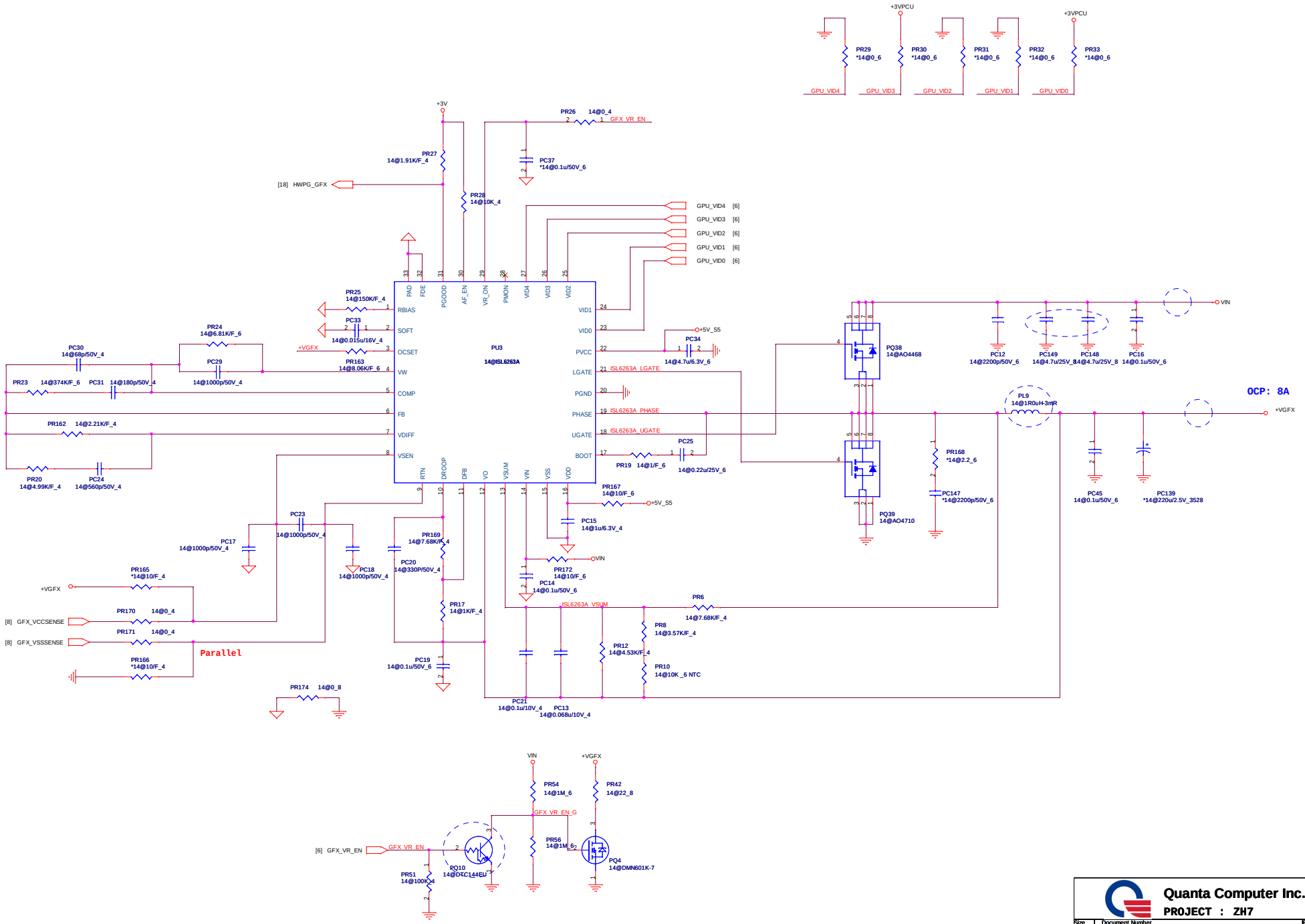

Quanta Computer Inc.		
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Model	REV	CHANGE LIST
ZH7 MB	1A	FIRST RELEASED: (PCB:A)
	2B	Page 2 : No Stuff R162 FOR EMI Page11 : Remove R282 ,R36 & R39 Page11 : Change CN14 footprint. Page14 : Remove D7 Page17 : Change Q15 frome 2N7002 to DTC144EU for speaker funcation. Page17 :Stuff U15, R244 & R227 , No stuff L23 for audio noisy. Page18 : Add R324 Page18 : Add R323 Page19 : Add R325 and short to CN11.44 for 3G LED function Page19 : Remove 3G wake up funcation ,Remove R179 , R183 & U11 Page20 : CN9 Change pin define.(CONN. reverse) Page 9 ,13 ,17 ,22 ,23 &25 : R116 ,R269 ,R74 ,R92 ,C330 ,C349 ,R211 ,R220 ,R231 ,R243 ,R248 &R317 Change to short pad Page 18 : D5 ,D20 & D13 Change footprint. Page 29 : PL9 Change footprint. Page 3 : R142 Change footprint. Page 25 : PU10 Change footprint. Page 11 : CN14 Change footprint. Page 21 : CN4 Change footprint.
	3C	Page 17 ,20 ,21 & 22 : R186 ,R187 ,R188 ,R189 ,R241 ,R196 ,R315 ,R20 & R316 Change to short pad Page 18 : Add R321 for ESD(Vedor suggest) Page 18 : D21 connect to HWPG_GFX Page 18 : D29 replace by R323. Page 20 : DEL R6 ,R7 & L2 Page 21 : CN2 connect to 3G_MINI2_LED meet customer request. and add C430 for EMI Page 22 : CN3.21 Change to floating Page 25 : page25 Delete PC127;PC128 10uf/25V_1206 and add PC164 100uF/25V 6x5.7 Page 27 : Add PC163 100uF/25V 6x5.7 Page 28 : Add R323 and R327
	1D	

MODEL	ZH7 FROM	ZH7 To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
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	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A

Quanta Computer Inc.
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DOC NO.	PROJECT MODEL :	ZH7	APPROVED BY:		DATE:	2008/12/05
	PART NUMBER:		DRAWING BY:		REVISON:	1A

EC GPIO Setting

Pin Name	Net Name	Setting	Description
GPIO1	ACIN	GPI	EC Detect AC Adapter State
GPIO3	NBSWON#	GPI	Pwer switch in
GPIO4/AD5		GPI	No used
GPIO5/AD4		GPI	No used
GPIO6	LID#	GPI	Reserved for Lid function
GPIO7	SUSB#	GPI	S.B sleep S3 pin
GPIO10/LPCPD#		GPI	No used
GPIO11/CLKRUN#	CLKRUN#	O	Clock Run
GPIO12/PSDAT3	KILL_SW_BT#	GPI	Detect bule tooth enable/disable
GPIO13/C_PWM	PWRLED#	O	Power on LED drive
GPIO14/TB1	FANSIG	GPI	To detect FAN speed
GPIO15/A_PWM	CONTRAST	O	EC PWM for Panel Brightness
GPIO16/CIRTX		GPI	No used
GPIO17/SCL1	MBCLK	O	SMBus Clock for M/B
GPIO20/TA2		GPI	No used
GPIO21/B_PWM	NUMLED#	O	Number Lock LED drive
GPIO22/SDA1	MBDATA	I/O	SMBus Data for M/B
GPIO23/SCL3	3ND_MBCLK	O	SMBus Clock for acer ID flash
GPIO24/LDRQ#	EC_FPBACK#	GPO	Panel back light control
GPIO25/PSCLK3	MAINON	GPO	Turn On/Off main power
GPIO26/PSCLK2		GPI	No used
GPIO27/PSDAT2	BT_POWERON#	GPO	Turn On/Off bule tooth power
GPIO30/CIRTX2		GPI	No used
GPIO31/SDA3	3ND_MBDATA	I/O	SMBus Data for acer ID flash
GPIO32/D_PWM	BATLED0#	GPO	Battery status LED drive
GPIO33/H_PWM	BATLED1#	GPO	Battery status LED drive
GPIO34/CIRRXL		GPI	No used
GPIO35/PSDAT1	TPDATA	O	PS/2 data for touch pad
GPIO36/TB3	VRON	GPO	Turn On/Off CPU Power
GPIO37/PSCLK1	TPCLK	O	PS/2 clock for touch pad
GPIO40/F_PWM	SUSLED	GPO	S3 state LED drive
GPIO41	3G_WAKE_2	GPI	3G wake up
GPIO42/TCK		GPI	No used
GPIO43/TMS	AMP_MUTE#	GPO	Turn On/Off Audio Amplier
GPIO44/TDI		GPI	No used
GPIO45/E_PWM	CPUFAN#	O	EC PWM for Fan Module
GPIO46/cirrxm/trst#	3G_WAKE_1	GPI	3G wake up
GPIO47/SCL4		GPI	No used
GPIO50/TDO	D/C#	GPO	Battery charge / discharge control
GPIO51/TA3	S5_ON	GPO	Turn On/Off S5 Power plane
GPIO52/cirtx2/trdy#	PCIE_WAKE#_EC	GPI	No used
GPIO53/SDA4	EC_SCI#	O	EC SCI
GPIO54/ECSCI#	ECDB_CLOCK	GPI	No used
GPIO55/CLKOUT	ECDB_CLOCK	GPI	No used
GPIO56/TA1		GPI	No used
GPIO57/KBSOUT17	KILL_SW_WL#	GPI	Detect mini card 1 (WLAN) enable/diable
GPIO60/KBSOUT16	KILL_SW_3G#	GPI	Detect mini card 2 (3G) enable/diable
GPIO61/KBSOUT15	MY15	O	Keyboard scan output
GPIO62/KBSOUT14	MY14	O	Keyboard scan output
GPIO63/KBSOUT13	MY13	O	Keyboard scan output
GPIO64/KBSOUT12	MY12	O	Keyboard scan output
GPIO65/SMI#	EC_SMI#	O	EC SMI
GPIO66/G_PWM	CAPSLED#	O	Caps Lock LED drive
GPIO67/PWUREQ	USB_EN#	GPO	USB power enable/disable
GPIO70/IRRX2_IRSL0	SUSC#	GPI	S.B sleep S4 pin
GPIO71/IRTX/SOUT2	PWROK_EC	GPO	System Power Good for PCI Reset
GPIO72/IRRX1/SIN2	EC_RSMRST#	GPO	S.B Resume Power Reset
GPIO73/SCL2	2ND_MBCLK	O	SMBus Clock for CPU thermal
GPIO74/SDA2	2ND_MBDATA	I/O	SMBus Data for CPU thermal
GPIO75/SPI_SCK	PCI_RESET	GPO	PLTRST# enable/diable for mini card 2
GPIO76/SPI_DO/SHBM	3G_EN	GPO	Mini card 2 (3G) enable/disable
GPIO77/SPI_DI	CRT_SENSE#	GPI	To detect CRT
GPIO81	DNBSWON#	GPO	S.B Power button Event
GPIO82/TRIS#		GPI	No used
GPIO83/SOUT_CR/BADDR1	uR_SOUT_CR	GPI	No used (Address Setting)
GPIO84/BADDR0	BADDR0	GPI	No used (Address Setting)
GPIO87/CIRRRXM/SIN_CR	RF_EN	GPO	Mini card 1 (WLAN) enable/disable
GPIO90/AD0	TEMP_MBAT	I	EC detect battery state
GPIO91/AD1		GPI	No used
GPIO92/AD2	TPD_TRIP	GPI	No used
GPIO93/AD3	ICMNT	I	EC detect system current in AC mode
GPIO94/DA0		GPI	No used
GPIO95/DA1		GPI	No used
GPIO96/DA2		GPI	No used
GPIO97/DA3		GPI	No used

ICH9M GPIO Setting

Pin Name	Power	ICH9M Default	Net Name	Description	Setting	Internal PU/PD	External PU/PD
GPIO0/PMSYNC#	Core	GPI	PM_SYNC#	Power Management Sync	O		
GPIO1	Core	GPI	EC_SMI#	EC SMI	GPI		PU 10KΩ to +3V
GPIO2/PIRQE#	Core	GPI	INTE#	No used	GPI		PU 10KΩ to +3V
GPIO3/PIRQF#	Core	GPI	INTF#	No used	GPI		PU 10KΩ to +3V
GPIO4/PIRQG#	Core	GPI	INTG#	No used	GPI		PU 10KΩ to +3V
GPIO5/PIRQH#	Core	GPI	INTH#	No used	GPI		PU 10KΩ to +3V
GPIO6	Core	GPI	LID#_ICH	Lid function	GPI		PU 10KΩ to +3V
GPIO7	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO8	S5	GPI	EC_SCI#	EC SCI interrupt	GPI		PU 10KΩ to +3V_S5
GPIO9/WOL_EN	S5	Native	ICH_GPIO9	No used	GPI		PU 10KΩ to +3V_S5
GPIO10/SUS_PWR_ACK	S5	GPI	ICH_GPIO10	No used	GPI		PU 10KΩ to +3V_S5
GPIO11/SMBALERT#	S5	Native	ICH_GPIO11	No used	GPI		PU 10KΩ to +3V_S5
GPIO12/LAN_PHY_PWR_CTRL	S5	GPO	ICH_GPIO12	No used	GPI		PU 10KΩ to +3V_S5
GPIO13	S5	GPI	ICH_GPIO13	No used	GPI		PU 10KΩ to +3V_S5
GPIO14/AC_PRESENT	S5	GPI	ICH_GPIO14	No used	GPI		PU 10KΩ to +3V_S5
GPIO15/STP_PCI#	S5	Native	PM_STPPCI#	Stop PCI Clock	O		
GPIO16/DPRSLPVR	Core	Native	DPRSLPVR	Deeper Sleep-Voltage Regulator	O	PD 20KΩ	
GPIO17	Core	GPI	BORAD_ID0	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO18	Core	GPO	BORAD_ID1	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO19/SATA1GP	Core	GPI	ICH_GPIO19	No used	GPI		PU 10KΩ to +3V
GPIO20	Core	GPO		No used	GPO	PD 20KΩ	
GPIO21/SATA0GP	Core	GPI	BORAD_ID2	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO22/SCLOCK	Core	GPI	BORAD_ID3	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO23/LDRQ1#	Core	Native		No used	GPI	PU 20KΩ	
GPIO24/MEM/LED	S5	GPO		No used	GPO		
GPIO25/STP_CPU#	S5	Native	PM_STPCPU#	Stop CPU Clock	O		
GPIO26/S4_STATE#	S5	Native		No used	GPO		
GPIO27	S5	GPO		No used	GPO		
GPIO28	S5	GPO		No used	GPO		
GPIO29/OC5#	S5	Native	USBOC5#	No used	GPI		PU 10KΩ to +3V_S5
GPIO30/OC6#	S5	Native	USBOC6#	No used	GPI		PU 10KΩ to +3V_S5
GPIO31/OC7#	S5	Native	USBOC7#	No used	GPI		PU 10KΩ to +3V_S5
GPIO32/CLKRUN#	Core	GPO	CLKRUN#	PCI Clock Run	I		PU 8.2KΩ to +3V
GPIO33/HDA_DOCK_EN#	Core	GPO		No used	GPO	PU 20KΩ	
GPIO34/HDA_DOCK_RST#	Core	GPO		No used	GPO		
GPIO35/SATACLKREQ#	Core	GPO	CLKREQ#_SATA	SATA Clock Request	O		PU 10KΩ to +3V
GPIO36/SATA4GP	Core	GPI	ICH_GPIO36	No used	GPI		PU 10KΩ to +3V
GPIO37/SATA5GP	Core	GPI	ICH_GPIO37	No used	GPI		PU 10KΩ to +3V
GPIO38/SLOAD	Core	GPI	ICH_GPIO38	No used	GPI		PD 10KΩ to GND
GPIO39/SDATAOUT0	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO40/OC1#	S5	Native	USBOC1#	No used	GPI		PU 10KΩ to +3V_S5
GPIO41/OC2#	S5	Native	USBOC2#	No used	GPI		PU 10KΩ to +3V_S5
GPIO42/OC3#	S5	Native	USBOC3#	No used	GPI		PU 10KΩ to +3V_S5
GPIO43/OC4#	S5	Native	USBOC4#	No used	GPI		PU 10KΩ to +3V_S5
GPIO44/OC8#	S5	Native	USBOC8#	No used	GPI		PU 10KΩ to +3V_S5
GPIO45/OC9#	S5	Native	USBOC9#	No used	GPI		PU 10KΩ to +3V_S5
GPIO46/OC10#	S5	Native	USBOC10#	No used	GPI		PU 10KΩ to +3V_S5
GPIO47/OC11#	S5	Native	USBOC11#	No used	GPI		PU 10KΩ to +3V_S5
GPIO48/SDATAOUT1	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO49	Core	GPO	DMI_TERM_SEL	No used	GPO	PU 20KΩ	
GPIO50/REQ1#	Core	Native	REQ1#	No used	GPI		PU 10KΩ to +3V
GPIO51/GNT1#	Core	Native		No used	GPI	PU 20KΩ	
GPIO52/REQ2#	Core	Native	REQ2#	No used	GPI		PU 10KΩ to +3V
GPIO53/GNT2#	Core	Native		No used	GPI	PU 20KΩ	
GPIO54/REQ3#	Core	Native	REQ3#	No used	GPI		PU 10KΩ to +3V
GPIO55/GNT3#	Core	Native		No used	GPI	PU 20KΩ	
GPIO56	S5	GPI	ICH_GPIO56	No used	GPI		PU 10KΩ to +3V_S5
GPIO57	S5	GPI	ICH_GPIO57	No used	GPI		PD 100KΩ to GND
GPIO58/SPI_CS1#	S5	GPI	SPI_CS1#	No used	GPI	PU 20KΩ	
GPIO59/OC0#	S5	Native	USBOC0#	No used	GPI		PU 10KΩ to +3V_S5
GPIO60/LINKALERT#	S5	Native	ICH_GPIO60	No used	GPI		PU 10KΩ to +3V_S5

CK505 Clock Setting Table

Differential CPU Clock

Pin Name	Pin	Net Name	Description
CPU_0	61	CLK_CPU_BCLK	
CPU_0#	60	CLK_CPU_BCLK#	Differential CPU clock
CPU_1	58	CLK_MCH_BCLK	
CPU_1#	57	CLK_MCH_BCLK#	Differential NB GS45 clock

PCI Express Clock

Pin Name	Pin	Net Name	Description
SRC0/DOT96	20	DREFCLK	
SRC0#/DOT96#	21	DREFCLK#	96MHz DOT clock for NB GS45
LCDCLK/27M	24	DREFSSCLK	
LCDCLK#/27M_SS	25	DREFSSCLK#	Clock output for NB GS45 graphic contoller
SRC2	28	PECLK_SATA	
SRC2#	29	PECLK_SATA#	Differential Serial Reference Clock for SB ICH9M SATA
SRC3/CR#_C	31	PECLK_ICH	
SRC3#/CR#_D	32	PECLK_ICH#	Differential Serial Reference Clock for SB ICH9M
SRC4	34	PECLK_LAN	
SRC4#	35	PECLK_LAN#	Differential Serial Reference Clock for on board LAN
SRC6	48	PECLK_MINI2	
SRC6#	47	PECLK_MINI2#	Differential Serial Reference Clock for Mini Card 2
SRC7/CR#_F	51		No use
SRC7#/CR#_E	50	CLKREQ#_MINI2	Clock Request for Mini Card 2 (SRC6)
SRC8/CPU_ITP	54		
SRC8#/CPU_ITP#	53		No use
SRC9	37	PECLK_MINI1	
SRC9#	38	PECLK_MINI1#	Differential Serial Reference Clock for MINI CARD 1
SRC10	41	PECLK_3GPLL	
SRC10#	42	PECLK_3GPLL#	Differential Serial Reference Clock for NB GS45
SRC11/CR#_H	40	CLKREQ#_MCH	Clock Request for NB GS45 (SRC10)
SRC11#/CR#_G	39	CLKREQ#_MINI1	Clock Request for Mini Card 1 (SRC9)

PCI Clock

Pin Name	Pin	Net Name	Description
PCI0/CR#_A	8	CLKREQ#_SATA	Clock Request for SATA (SRC2)
PCI1/CR#_B	10	CLKREQ#_LAN	Clock Request for on board LAN (SRC4)
PCI2	11	PCLK_DEBUG	PCI clock for debug card
PCI3	12		No use
PCI4	13	PCLK_EC	PCI clock for EC
PCI5	14	PCLK_ICH	PCI clock for SB ICH9M

Other Clock

Pin Name	Pin	Net Name	Description
USB_48	17	CLK48_ICH	48MHz for SB ICH9M
		CLK48_CARD	48MHz for USB Card Reader
REF	5	CLK14_ICH	14.318MHz for SB ICH9M

Clock Request Table

CLKREQ#	MAPPING		Control
	0	1	
CR#_A	SRC0	SRC2	SATA
CR#_B	LCDCLK	SRC4	LAN
CR#_C	SRC0	SRC2	N/A
CR#_D	LCDCLK	SRC4	N/A
CR#_E	SRC6		MINI2
CR#_F	SRC8		N/A
CR#_G	SRC9		MINI1
CR#_H	SRC10		MCH

QUANTA COMPUTER

Title: **Schematic Setting**

Size	Document Number	Rev
	ZH7	0C

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